Dynamic Modelling of VSCs in a *dq* Rotating Frame for Pole-to-Pole dc Fault Study

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Abstract: As the future dc grids will involve numerous converter systems, the accuracy and speed of their modelling becomes of high importance. The modelling in a rotating *dq* frame is able to transform the quantities from ac variables to dc variables resulting in significantly improved simulation speed. *dq* analytical modelling is normally used only for dynamic studies with voltage source converter (VSC), while large-disturbance dc faults are commonly studied in static *abc* frame. A new *dq* frame modelling method for VSC, including MMC topology, for dc fault study is proposed. A unified modelling of the VSC for both dynamic and dc fault study is therefore developed. The model is separately presented for other fault-tolerant VSC, like LCL VSC. Simulation results verified that the proposed model is accurate when compared with detailed switching model on PSCAD/EMTDC. The proposed unified VSC model is able to replace the detailed switching model for both dc fault (only pole-to-pole dc fault is studied) and dynamic studies. The modelling approach opens the possibility for modelling large dc grids in *dq* frame for wide range of operating conditions.

1 Introduction

With the development of voltage source converter (VSC) and renewable technology, there has been significant interest in developing multi-terminal HVDC system and establishing dc grids [1]. Micro dc grid has also attracted significant attention [2]. In all such dc grids, numerous VSCs will be used with possible additional dc/dc converters. How to efficiently simulate such system is a big challenge.

Electro-magnetic transient simulation is a typical way of studying such systems with ac/dc converters [3]. As the number of employed VSCs is large, the simulation time will become unacceptable if all these VSCs are modelled using detailed switching methods [4]-[5].

An alternative way is to neglect the switching transitions of power semiconductors and represent the ac voltage of a converter bridge using a controlled voltage source at fundamental frequency[4]-[5]. This method is called AVM (average value modelling) and it is usually implemented in the static *ABC* frame. Typically, all the ac quantities are represented as ac oscillating variables.

The AVM model in the *ABC* frame is not feasible if medium frequency components operating at the frequency of 500Hz-2kHz are employed in a dc grid, such as the medium frequency dc-dc converters reported in [6]-[8]. Here we have 1-3kHz fundamental frequency in the inner ac circuit. The required

simulation step would be around 1μs-5 μs even if the AVM in the *ABC* frame is employed. Simulation step for the whole dc grid must be the same as for the slowest converters and this becomes unacceptably slow when complex dc grids are studied.

To solve the challenge of efficient AVM modelling, a possible approach is to model all the ac quantities in a rotating *dq* frame. All the ac variables will then become dc variables in the *dq* frame, the simulation step could therefore be increased, and studies have shown that such models can increase simulation speed perhaps two orders of magnitude [9]. Also, dq frame modelling facilitates linearization resulting in models suitable for eigenvalue studies.

However, the modelling of VSCs in the rotating *dq* frame is typically applied only to analytical dynamic studies and controller design [10], [11]. IGBTs of common *L*-VSCs or half bridge MMC (Modular Multilevel Converter) are blocked during dc faults, and the converter becomes a diode bridge in such case. The studies under dc faults and large disturbances are typically performed in ABC frame simulation platforms [12]-[14]. There have been no reported studies on modelling a VSC in a rotating *dq* frame for dc fault studies.

dq frame modelling may become prevalent with large dc grids because of complexity of the grid, and since numerous converters are used. In such case it is important to extend dq modelling to dc fault conditions; since transient fault current magnitudes (both on dc and ac sides) are important for component dimensioning. Some converters retain control during dc faults since they can limit dc fault current [15]. For the same fault, some other VSCs in a dc grid might be blocked and the overall dynamics and stability of faulted dc grid are of interest [16].

An intuitive way of modelling VSC during dc fault is to model the blocked VSC (a diode bridge) following the common modelling approach of current source converter with zero ignition angle delay [17]-[18]. Such method is however found to be inaccurate in this paper, as also reported in [19]-[20]. References [19]-[20] presented the modelling of three-phase diode bridge connected to synchronous generator. Because of the complexity of the main generator's and exciter's ac variables' waveforms, the coefficients in the AC/DC link equations cannot be found analytically but only using experiments under different load levels. Also, modelling of diode bridge under dc fault was not discussed in [19]-[20].

Dynamic analytical modelling of a diode bridge connected to dc load was proposed in [21]. Nevertheless this model also uses common diode rectifier with dc inductors, which operates as a current source converter and furthermore dc fault condition is not considered.

To enable accurate dq frame VSC modelling in blocked state (under dc faults), a new modelling method was proposed in [22] and will be further developed in this paper. We aim advancing work in [22]

for wide range of conditions, and developing integrated VSC model in DQ frame that incorporates both normal operation and blocked state.

2 Studied VSCs and overall modelling structure

2.1 The studied VSCs

Fig. 1 (a) shows the circuit diagram of the studied *L*-VSC. The ac side is modelled by an ac voltage source in series with resistor R_s and inductor L_s. The *L*-VSC is interfaced to the PCC (point of common coupling) through transformer/phase inductor. The transformer/phase inductor is modelled by R_k, L_k in series with an ideal transformer with turn ratio k_t. v_s is the voltage of the remote ac source, v is the voltage at PCC, v_{con} is the ac voltage of the converter scaled to the grid side of ac transformer. θ is the angle of v referred to v_s and θ_m is the angle of modulation indices referred to the angle of v, which assumes that PLL (Phase Locked Loop) tracks v. Fig. 1 (b) shows the circuit diagram of dc fault tolerant LCL-VSC [16], which will also be modelled under dc faults in section 5. Modelling of MMC with its IGBTs blocked will also be studied in section 5.

2.2 Selection of the rotating frames

A rotating *xy* frame with its angle aligned with the phase *A* voltage of the voltage source (v_{sA}) and a rotating *dq* frame with its angle aligned with the voltage at PCC are respectively used to model the ac circuit and the control system of a VSC. Explanation of employing two rotating frames is given as below:

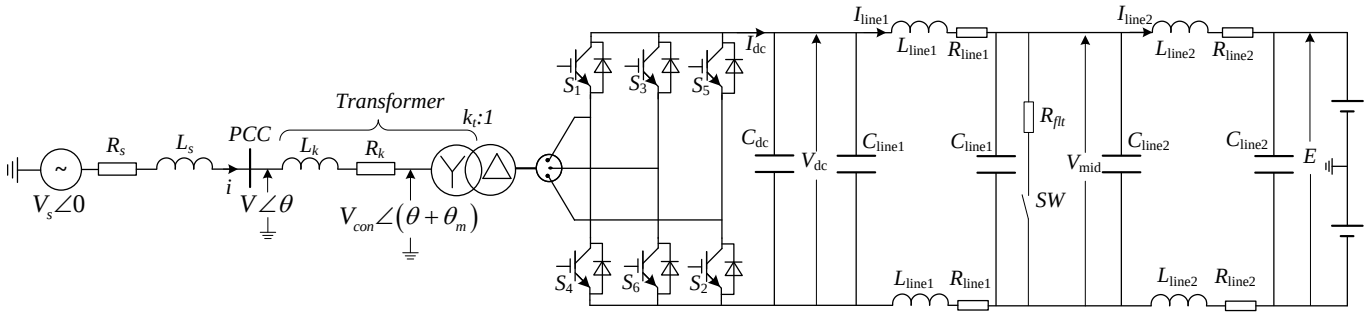
Normally, a *dq* rotating frame is positioned at the PCC for control of the VSC. With the changes of the operating point of VSC, phase angle difference between the PCC *dq* frame and the angle of v_s also changes. If the PCC *dq* frame is also used to model the dynamics of the ac circuits, the *dq* components of v_s becomes variables in the PCC *dq* frame. While in the modelling, *dq* components of v_s should be fixed values as v_s is an external fixed electrical input, magnitude and phase angle of v_s are fixed and do not depend on the control system.

Fig. 2(a) demonstrates the frames involved in this paper. The *d*-axis is plotted to be lagging the PCC voltage vector $\overline{V}$. In a real system, such lagging only happens during transients. The VSC controller and the control signals M_d+jM_q are based on the local *dq* frame and need to be transformed to the global *xy* frame for the state-space modelling. Similarly, the measurements such as V_x+jV_y, I_x+jI_y are based on the global *xy* frame, and they need to be transformed to the *dq* frame for control purpose. Two sample equations for converting the variables between these two frames are demonstrated as:

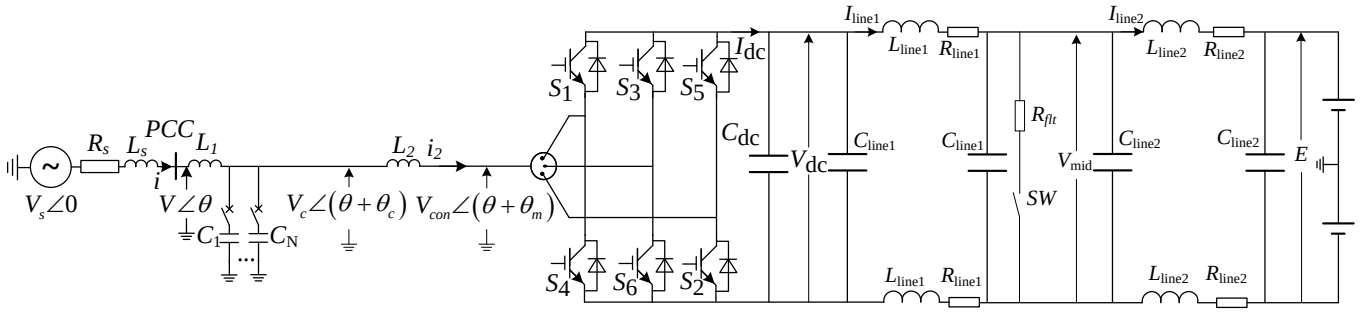
$$M_x + jM_y = (M_d + jM_q)e^{j\theta}$$
$$= (M_d \cos\theta - M_q \sin\theta) + j(M_d \sin\theta + M_q \cos\theta) \quad (1)$$

$$V_d + jV_q = (V_x + jV_y)e^{j(-\theta)}$$
$$= (V_x \cos\theta + V_y \sin\theta) + j(V_y \cos\theta - V_x \sin\theta) \quad (2)$$

Where subscripts *d* and *q* denote *dq* frame and subscripts *x* and *y* denote *xy* frame.

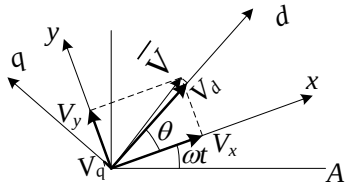


(a) Circuit diagram of an L-VSC

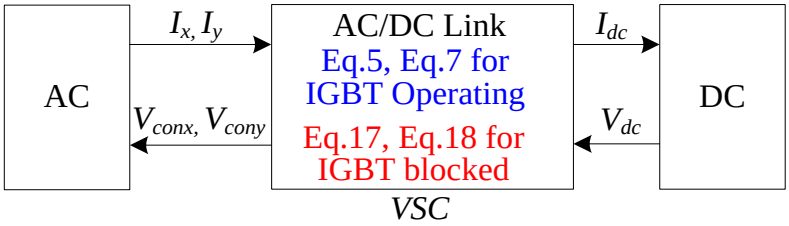


(b) Circuit diagram of an LCL-VSC

Fig. 1 Circuit diagrams of the studied systems



(a) Selection of the rotating frames



(b) Unified 2-level VSC model structure for both IGBT operating and IGBT blocked scenarios

Fig. 2 Selection of the rotating frames and the unified modelling structure

2.3 Modelling of operating VSC in dq Frame for dynamic study

With the *x-axis* positioned at the source voltage V_{sx}, the equations for the ac circuit of Fig. 1(a) are:

$$\frac{d}{dt}I_x = \frac{1}{L_{tot}}(V_{sx} - V_{conx} - R_{tot}I_x + \omega L_{tot}I_y) \qquad (3)$$

$$\frac{d}{dt}I_y = \frac{1}{L_{tot}}(-V_{cony} - R_{tot}I_y - \omega L_{tot}I_x) \qquad (4)$$

Where $L_{tot}=L_s+L_k$, $R_{tot}=R_s+R_k$. In (1)-(3), I_x, I_y are selected as state variables, V_{sx} is the electrical input, $V_{sy}=0$ and is not provided in (4), V_{conx} and V_{cony} are the ac voltages of the VSC viewed at the grid side of the transformer, ω is the angular frequency of the ac circuit. V_{conx}, V_{cony} and I_{dc} are calculated from the state variables using the following equations [11],

$$V_{conx} = k_t k_m M_x \frac{V_{dc}}{2}, V_{cony} = k_t k_m M_y \frac{V_{dc}}{2} \qquad (5)$$

Where k_t is the transformer turn ratio as indicated in Fig. 1(a), k_m is a coefficient related to the modulation method. $k_m=1$ if employing the typical PWM modulation with L-VSC.

Equation for the active power balance is

$$\frac{3}{2}(V_{conx}I_x + V_{cony}I_y) = V_{dc}I_{dc} \qquad (6)$$

Substitute (5) into (6), the following link equation for ac and dc currents is derived,

$$I_{dc} = k_t k_m \frac{3}{4}(M_x I_x + M_y I_y) \qquad (7)$$

The dc transmision line is modelled by two PI sections. The PI section constructs by C_{line1}, L_{line1} and R_{line1} represents the PI section from dc terminal of the VSC to the fault point and the PI section constructed by C_{line2}, L_{line2} and R_{line2} represents the PI section from the dc fault point to external dc votlage source. Modelling of the dc circuit in normal condition gives:

$$\frac{d}{dt}V_{dc} = \frac{1}{C_{dc}+C_{line1}}(I_{dc} - I_{line1}) \qquad (8)$$

$$\frac{d}{dt}I_{line1} = \frac{V_{dc} - V_{mid} - 2R_{line1}I_{line1}}{2L_{line1}} \qquad (9)$$

$$\frac{d}{dt}V_{mid} = \frac{1}{C_{line1} + C_{line2}}(I_{line1} - I_{line2}) \qquad (10)$$

$$\frac{d}{dt}I_{line2} = \frac{V_{mid} - E - 2R_{line2}I_{line2}}{2L_{line2}} \qquad (11)$$

Definitions of the variables shown in (8)-(11) are illustrated in Fig. 1(a) and (b).

VSC model topology in normal operation is demonstrated in Fig. 2(b). The ac-model outputs are I_x, I_y which are used to calculate I_{dc} which is then passed to the dc side. The dc-model output is V_{dc} which is used to calculate V_{conx}, V_{cony} which is passed to the ac side.

3 Accuracy problems when modelling blocked VSC using CSC approach

IGBTs of a VSC will be blocked during dc faults, and a VSC becomes a diode bridge. Several textbooks have addressed the operating principles of a diode bridge [17]-[18]. However, in most of the diode bridge applications, there is a large inductor on dc side which keeps dc current constant and the diode bridge is treated in a similar way as a current source converter (CSC). On such assumption, the dc voltage is calculated from the ac voltage and dc current using the following equations [17]:

$$V_{dc} = \frac{3\sqrt{3}V^{peak}}{\pi k}(1 - \frac{\omega L_k I_{dc}}{\sqrt{3}V_P k}), \quad \mu < \pi/3 \qquad (Mode1) \quad (12)$$

Where μ is the commutation overlap of the diode bridge during dc fault, V^{peak} is the peak value of phase-ground ac voltage at the PCC, which is calculated by

$$V^{peak} = \sqrt{V_x^2 + V_y^2} \qquad (13)$$

Equation (12) is defined as operating *Mode1* of a diode bridge. The above equation considers the most common case where the commutation overlap of the diode bridge is less than π/3 [17],[19].

If μ equals to π/3, it indicates that there will be *3* diodes conducting at any time. The dc voltage is then calculated by[17].

$$V_{dc} = \frac{3V^{peak}}{\pi k}\frac{\sqrt{3}}{2}\frac{\sqrt{\left(V^{peak}\right)^2 - (2\omega L_k I_{dc}/k)^2}}{V^{peak}}, \quad \mu = \pi/3, \quad V_{dc} \geq 0 \quad (Mode2) \quad (14)$$

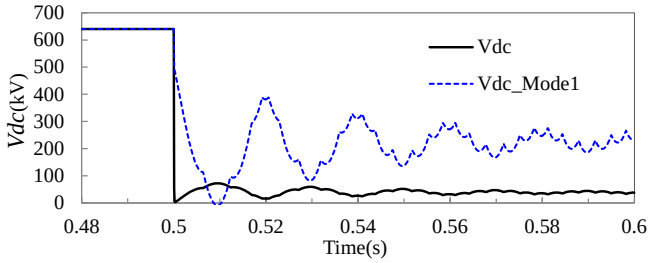
Equation (14) is defined as operating *Mode2* of a diode bridge and V_{dc} is a non-negative value.

Fig. 3 (a) and (b) compare dc fault response of detailed PSCAD model of the test L-VSC (parameters listed in Table 4) with its IGBT blocked and for simplicity L_{line1}=0. A pole-to-pole dc fault is applied at 0.5s. The value of V_{dc_mode1} before 0.5s is calculated from a VSC approach, which is the same as the value

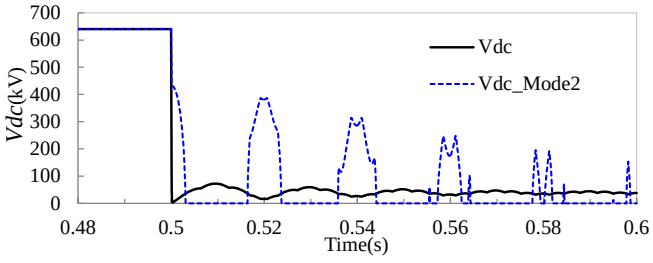
obtained from detailed PSCAD model and the value of V_{dc_mode1} after 0.5s is calculated using(12). We can see from Fig. 3 (a) that (12) is not able to accurately represent dc voltage during dc fault.

Fig. 3 (b) similarly compares the detailed PSCAD model and the dc voltage calculated (V_{dc_Mode2}) according to (14) and we can see that (14) is also not able to determine correct dc voltage. In Fig. 3 (b), the V_{dc_Mode2} is discontinuous as the dc voltage of a three-phase diode bridge always remain higher than 0.

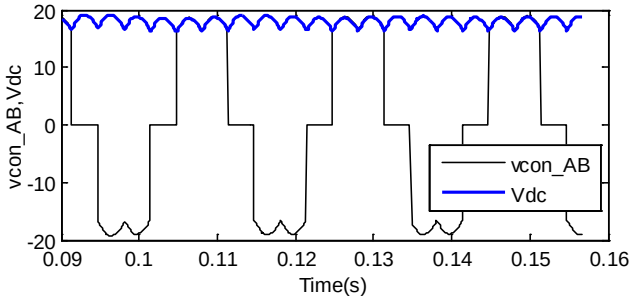
Another issue with current source diode bridge modelling is that such CSC model has different structure from VSC model in normal operation. The model structure from Fig. 2(b) does not apply since a current source diode bridge takes ac voltage and dc current as inputs and gives ac current and dc voltage as outputs.



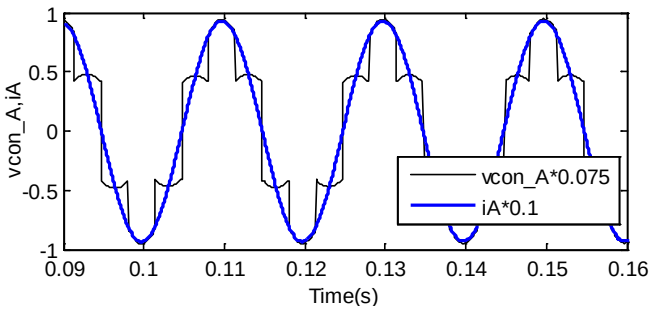
(a) Comparison of measured V_{dc} and the value calculated from (12)



(b) Comparison of measured V_{dc} and the value calculated from (14)



(c) Converter line-line voltage and dc voltage in steady state during a dc fault(detailed model R_{line1}=1Ω, R_{flt}=0.01Ω, L_{ine1}=0)



(d)Comparison the phase angle of i and v_{con} during a dc fault(detailed model R_{line1}=1Ω, R_{flt}=0.01 Ω, L_{ine1}=0)

Fig. 3 Voltage and current under different modelling approaches

4 Modelling of blocked VSC following VSC diode bridge approach

4.1 AC/DC link equations during dc fault

Because of the inductance and resistance between the dc terminals of a VSC to the dc fault point, and the resistance of diodes, the dc voltage seen at the converter bridge will never be exactly zero (in case that $V_{dc}=0$ a singularity occurs). The line-line ac voltage at the converter bridge will be 120° square-waves clamped at $\pm V_{dc}$, as seen in Fig. 3 (c). Peak value of the fundamental component line-line voltage is

$$V_{con\_LL}^{peak} = \frac{4}{\pi}\sin(\frac{\pi}{3})V_{dc} \quad (15)$$

Amplitude of the converter voltage vector $V_{conx}+jV_{cony}$ (line-neutral value) is derived from (15) as follows:

$$\sqrt{V_{conx}^2 + V_{cony}^2} = \frac{2}{\pi}V_{dc} \quad (16)$$

The angle of ($V_{conx}+jV_{cony}$) needs also to be calculated to get explicit expression of V_{conx} and V_{cony}. Since there is no inductance between $V_{conx}+jV_{cony}$ and the diodes as seen in Fig. 1, the commutation overlap (μ) of the diode bridge can be assumed zero. The angle of $V_{conx}+jV_{cony}$ is the same as the angle of I_x+jI_y, which is valid for any diode bridge. Since I_x and I_y are selected as state variables, V_{conx} and V_{cony} are therefore calculated by:

$$V_{conx} = \frac{2}{\pi}V_{dc}\frac{I_x}{\sqrt{I_x^2 + I_y^2}},\ V_{cony} = \frac{2}{\pi}V_{dc}\frac{I_y}{\sqrt{I_x^2 + I_y^2}} \quad (17)$$

Fig. 3 (d) compares the phase angle of i_A and v_{conA} for the test L-VSC of Table 4 with its IGBTs blocked in steady state using detailed switching model. Parameters of R_{flt}=0.01 Ω, L_{line1}=0 is used in the test of Fig. 3 (d).

To show the voltage waveform and current waveform in the same graph, the voltage is scaled by 0.075 and 0.1.It is seen that v_{conA} is in phase with i_A, which verifies the above derivations of (17).

Substitute (17) into (6), the dc current equation during dc fault (with nonzero V_{dc}) is:

$$I_{dc} = \frac{3}{\pi}\sqrt{I_x^2 + I_y^2} \quad (18)$$

4.2 Modelling of freewheeling stage

Because of the dc inductance present at the dc side of a VSC, the VSC diode converter may enter freewheeling state if dc voltage attempts to reverse [12]. Freewheeling state is characterised by two diodes on the same phase conducting simultaneously. This state gives zero dc voltage and prevents any negative dc voltage (diodes cannot conduct in reverse).

The freewheeling state should be accurately represented in the diode bridge dq model. However the expression in (8) may actually give unrealistic negative dc voltage depending how dynamics evolve in time domain.

It is therefore proposed to introduce zero as the lower limit on the integrator employed to solve dc voltage dynamics in (8). Therefore VSC diode bridge model becomes non-linear, where state variable in (8) is clamped to positive value:

$$\frac{d}{dt}V_{dc} = \frac{1}{C_{dc}+C_1}(I_{dc} - I_{line1}), \quad \mathrm{V_{dc}} \geq 0 \qquad (19)$$

A simplified linearized model can be used for diode bridge, by removing non-linear limit in (19), as long as dc voltage remains positive.

4.3 Unified VSC modelling structure considering both normal operation and dc fault state

In summary we propose a unified 2-level VSC model structure, as summarized in Fig. 2(b). Equations (5) and (7) are used to calculate V_{conx}, V_{cony} and I_{dc} in normal operation while (17)- (18) are used during dc fault.

On the dc side, during dc fault, V_{dc} stays the same as given in (8), while equation for dc line current I_{line1} needs to be changed as follows,

$$\frac{d}{dt}I_{line1} = \frac{V_{dc} - (2R_{line1} + R_{flt})I_{line1}}{2L_{line1}} \qquad (20)$$

Therefore eequation (9) is used for dc line current in normal operation and (20) is used for dc line current during dc fault.

5 Modelling of LCL-VSC and MMC for dc fault study

5.1 Modelling of LCL-VSC for dc fault study

In the LCL-VSC, no ac transformer is used [15]. The LCL-VSC is interfaced to the PCC through a LCL (inductor-capacitor-inductor) circuit L_2-C-L_1, as seen in Fig. 1(b). The capacitors can be divided into several groups and C is the total sum of each C_{i}, namely, $C = \sum_{i=1}^{N} C_i$, where N is the total number of group of capacitors.

The state space equations for the ac circuit are:

$$\frac{d}{dt}I_x = \frac{1}{L_{totC}}(V_{sx} - V_{cx} - R_{totC}I_x + \omega L_{totC}I_y) \qquad (21)$$

$$\frac{d}{dt}I_y = \frac{1}{L_{totC}}(-V_{cy} - R_{totC}I_y - \omega L_{totC}I_x) \quad (22)$$

$$\frac{d}{dt}I_{2x} = \frac{1}{L_2}(V_{cx} - V_{conx} - R_2 I_{2x} + \omega L_2 I_{2y}) \quad (23)$$

$$\frac{d}{dt}I_{2y} = \frac{1}{L_2}(V_{cy} - V_{cony} - R_2 I_{2y} - \omega L_2 I_{2x}) \quad (24)$$

$$\frac{d}{dt}V_{cx} = \frac{1}{C}(I_x - I_{2x} + \omega C V_{cy}) \quad (25)$$

$$\frac{d}{dt}V_{cy} = \frac{1}{C}(I_y - I_{2y} - \omega C V_{cx}) \quad (26)$$

Where $L_{totC}=L_s+L_1$, $R_{totc}=R_s+R_1$, V_{cx} and V_{cy} are the capacitor voltages in the xy frame. The dc side equations and AC/DC link equations for a LCL-VSC are exactly the same as **(8)-(9)**.

5.2 Active control of LCL-VSC during dc fault

According to [15] - [16], IGBT currents during dc fault are low and IGBTs of an LCL-VSC can remain conducting even during dc fault. According to (7), $I_{dc}= 3k_m(M_xI_x+M_yI_y)/4$ if IGBTs remain control during dc fault. If the modulation indices M_x and M_y are kept at zero during dc fault, the dc current injected from the ac side can be reduced to low values with theoretical ideal value of 0.

Such operating mode of an LCL-VSC was not disclosed in [15] or [16] and its benefit will be verified in the simulation part.

If IGBTs of a LCL-VSC remain conducting during dc fault, modelling of a LCL-VSC during dc fault will be exactly the same as modelling of a LCL-VSC in normal operation. Equations (21)-(26) are used to model the ac side of a LCL-VSC, (5) and (7) are used to model the AC/DC link equations, (9) and (20) are used to calculate the dc line current I_{line1} during normal operation and during dc fault.

If IGBTs of a LCL-VSC are blocked during dc fault, we only need to replace (5), (7) using (17) and (18), while the other equations are the same as in the previous paragraph.

5.3 Modelling of MMC converter during dc fault

Fig. 4 (a) shows the commonly known circuit diagram of a MMC converter after blocking IGBTs [11]. The submodule capacitors are bypassed and they will not discharge into dc fault. The primary difference compared with L-VSC is that dc bus capacitor C_{dc} is not present and the arm inductors L_{arm} are added.

Similarly as 2-level VSC, the line-line ac voltage behind each arm inductor is clamped at $\pm V_{dc}$, namely, V_{dc} for e_{AB1} and $-V_{dc}$ for e_{AB2}. As shown in Fig. 4 (a), e_{AB1} is the potential difference between the high voltage terminal of phase A upper arm inductor and lower voltage terminal of phase B lower arm inductor,

e_{AB2} is the potential difference between the lower voltage terminal of the phase A lower arm and the high voltage terminal of phase B upper arm inductor.

Because of the arm inductors, the line-line ac voltage will not be ideal 120° square-wave. Fig. 4(b) shows the line-line ac voltage at converter bridge (e_{AB1}) and the dc voltage. We can see that voltage in Fig. 4(b) resembles Fig. 3 (c) but is distorted because of arm inductors. Fig. 4(c) shows the waveform of e_{AB1} and current i_A. There is some phase difference between e_{AB1} and i_A, which is the result of absence of a firm dc voltage (capacitors) source. Such angle difference is neglected in this article.

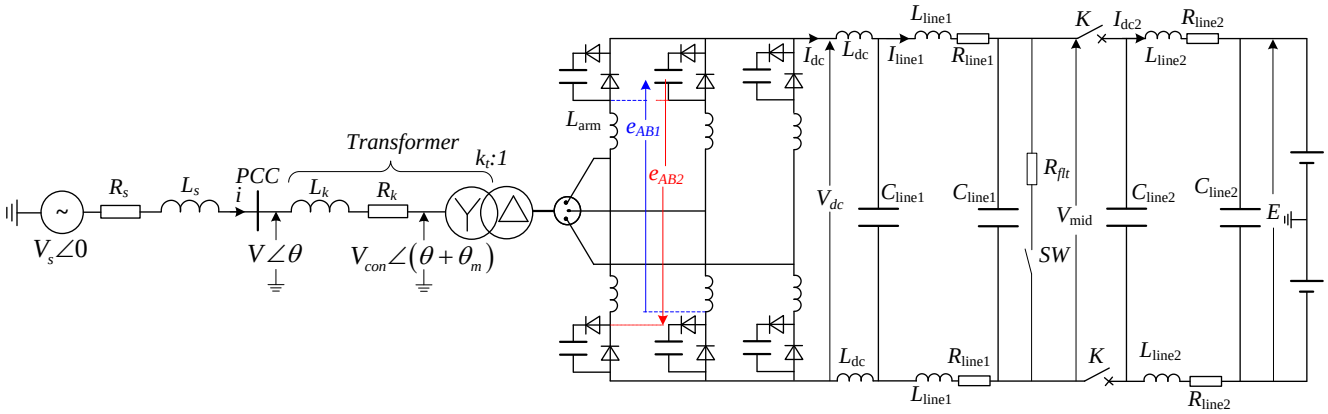
Fig. 4(d) shows the proposed modelling circuit of MMC after blocking IGBTs. Compared with 2-level VSC, arm inductor L_{arm} needs to be added to the ac circuit. The L_{tot} of (3)-(4) is changed to the following equation to include L_{arm}.

$$L_{tot} = L_s + L_k + k_t^2 L_{arm} \quad (27)$$

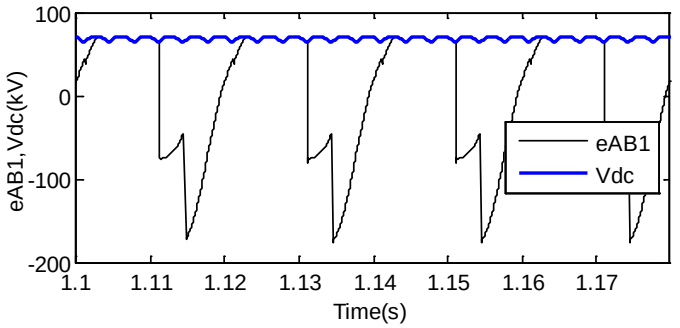
The same AC/DC link equations of (17)-(18) are used for a MMC with its IGBTs blocked.

It will be demonstrated in the simulation part that the above modelling approach for blocked MMC is very accurate for dc terminal voltage ≥ 20% of the rated dc voltage. For dc voltage lower than 20% the modelling approach becomes less accurate because of the highly distorted currents and voltages during dc fault. It has been demonstrated in [13] that because of current limiting reactors and in particular when the current limiting reactors associated with the fast acting dc circuit breakers are employed, the dc terminal voltage is typically higher than 35% the rated value (120kV for 320kV MMC [13]).

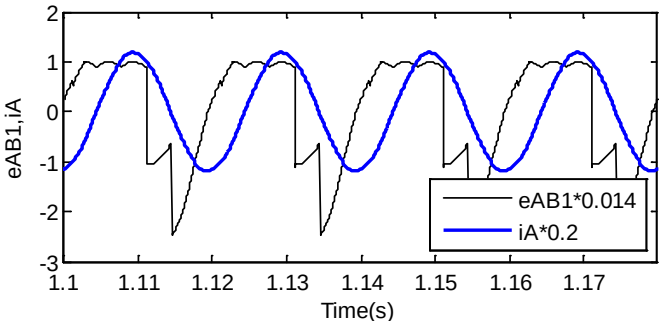
It should also be noted that the MMC converter has different *dq* frame model from 2-level VSC in normal operation [23]-[24]. Therefore with MMC VSC there will be transition of model topology between normal operation and diode bridge operation.



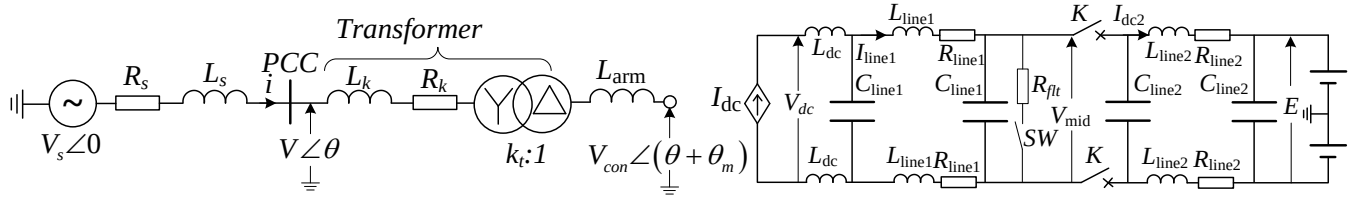
(a) Circuit diagram of a MMC after blocking IGBTs



(b) e_{AB1} and V_{dc}



(c) scaled e_{AB1} and i_A



(d) Equivalent model of MMC after blocking IGBTs

Fig. 4 Blocked MMC during a dc fault

6 L VSC Model Verification

6.1 Parameters of the tested L VSC

A test L-VSC with parameters listed in Table 2-Table 4 is used to verify the proposed modelling methods. Accuracy of the AVM under different values of L_{line1}=0.1H, 0.01H and 0.001H was tested. Accuracy of the AVM under lower dc fault impedance with R_{flt}=0.01Ω and under high impedance dc fault with R_{flt}=100 Ω is also tested, and confirmed. Only a limited number of tests will be shown.

6.2 Simulation of L VSC during low-impedance dc fault

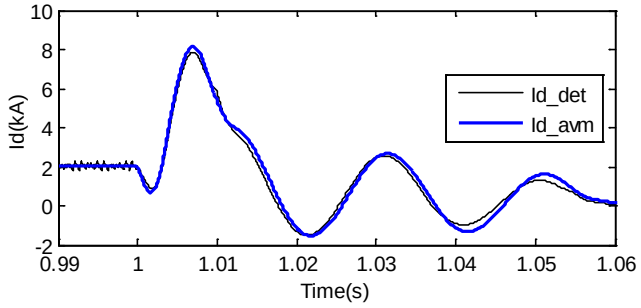
A pole-to-pole dc fault is applied at 1.0s by closing the switch *SW* in Fig. 1(a). Fig. 5(a)-(d), respectively, shows the *d*-channel ac current (i), *q*-channel ac current, dc current (I_{dc}) at the dc side of the converter bridge and pole-to-pole dc voltage (V_{dc}) at the dc terminals. Measuring points i, I_{dc} and V_{dc} are shown in Fig. 1(a). It is seen that the AVM in a rotating *dq* frame gives similar results as the detailed switching model in static ABC frame.

It is remarkable to notice that the dynamics during the first few milliseconds are well represented by the AVM.

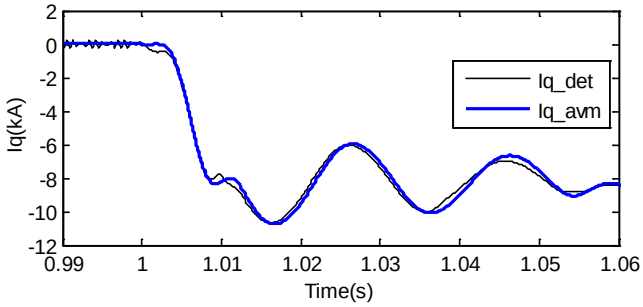
It is envisaged that the proposed modelling method is able to replace the conventional detailed switching model for both dynamics and dc-fault response study, if harmonics are not considered.

For application of the proposed VSC modelling in the future large dc grid, dc side of each VSC will be connected to the corresponding dc network model. In this study, the dc network is modelled as a dc battery in series with PI model dc transmission line, so as to enable detailed inspection of the VSC model.

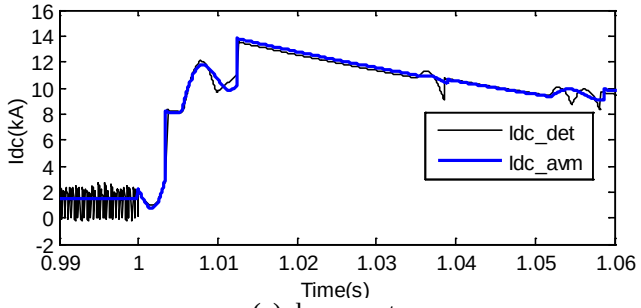
Fig. 6 shows simulation results with L_{line1}=0.001H. The simulation curves from AVM match the simulation curves from detailed switching model. Fig. 6(c) shows that peak value of the dc fault current significantly increase with the decrease of dc inductor. Such large dc fault current happens during the freewheeling stage in which both the upper diode and lower diode of a phase leg conduct [12].



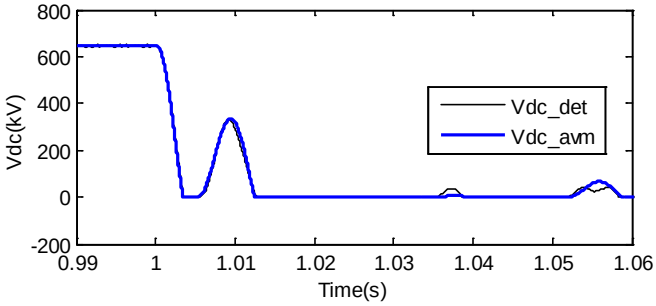
(a) *d*-channel current



(b) *q*-channel current

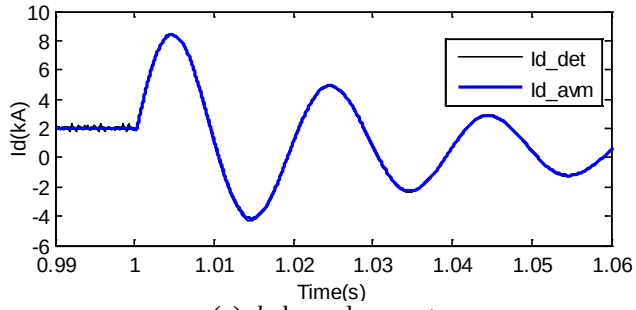


(c) dc current

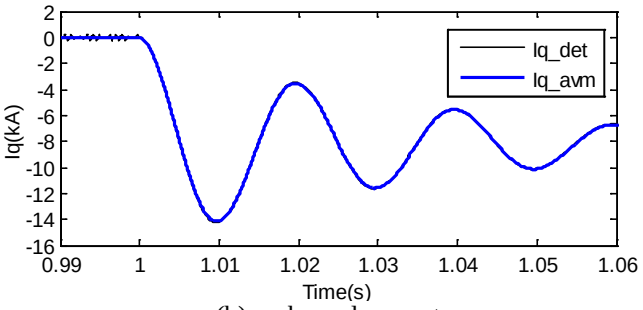


(d) dc voltage

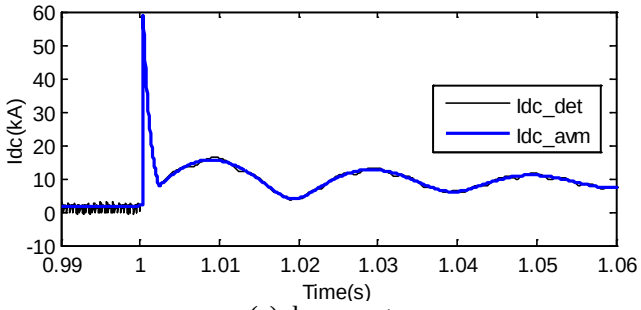
Fig. 5 Simulation of L-VSC with R_{flt}=0.01 Ω, L_{line1}=0.1H



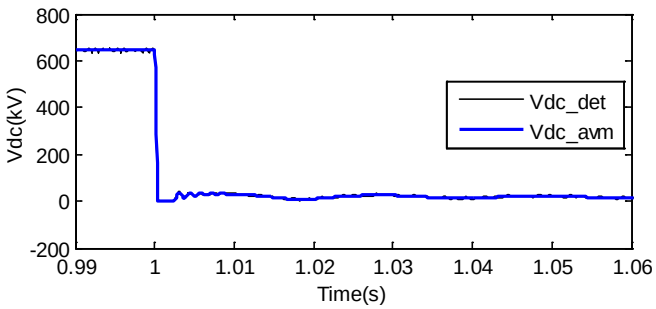
(a) *d*-channel current



(b) *q*-channel current



(c) dc current

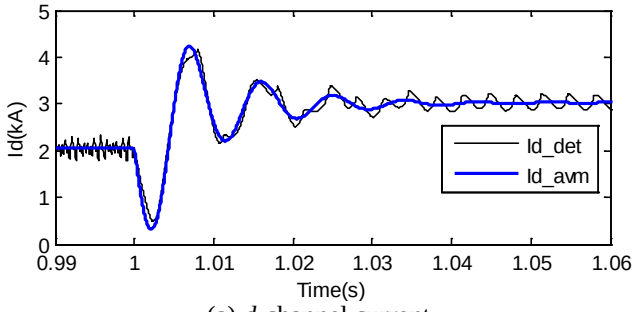


(d) dc voltage

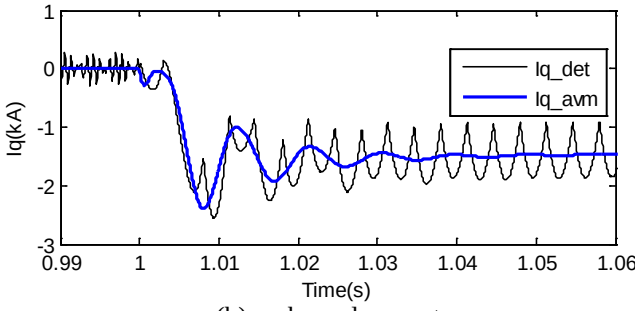
Fig. 6 Simulation of L-VSC with R_{flt}=0.01 Ω, L_{line1}=0.001H

6.3 Simulation of L VSC for high-impedance dc fault

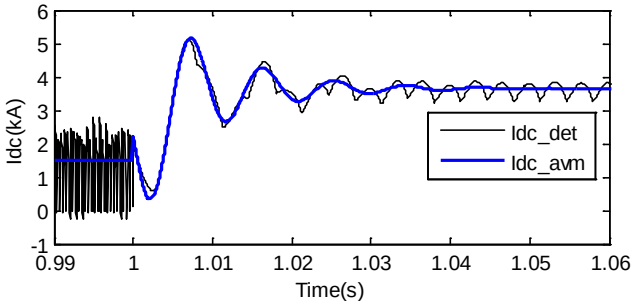
Fig. 7 shows the simulation of L-VSC under high-impedance dc fault (R_{flt}=100 Ω). It is seen that the dq frame model gives similar results as the detailed switching model even under high-impedance dc fault.



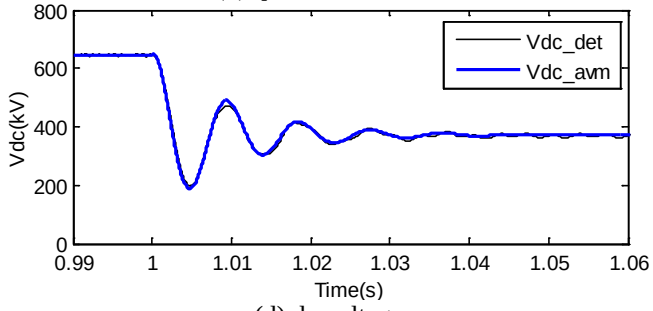
(a) *d*-channel current



(b) q-channel current



(c) dc current



(d) dc voltage

Fig. 7 Simulation of L-VSC with R_{flt}=100 Ω, L_{line1}=0.1H

7 LCL VSC Model Verification

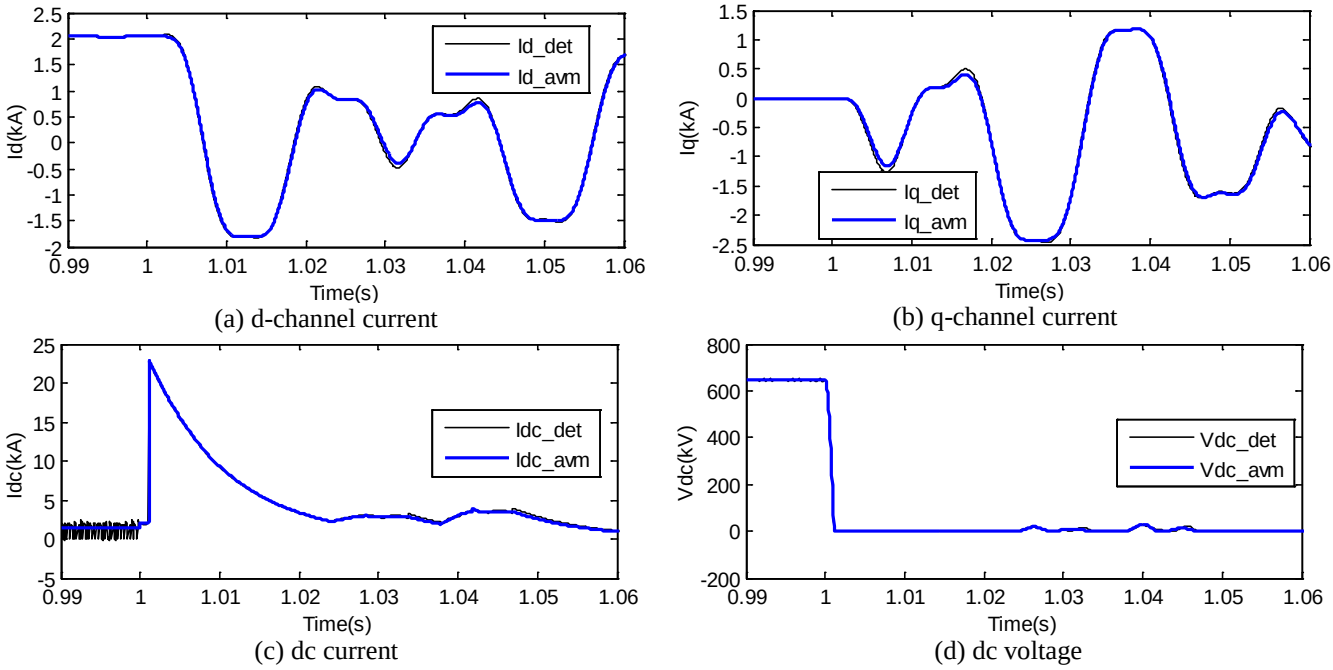
7.1 Parameters of the tested LCL VSC

A test LCL-VSC with parameters listed in Table 2-Table 3 and Table 5 is used to verify the proposed dq modelling of LCL-VSC. Accuracy of the AVM under dc fault with and without active control will be presented. Impacts of L_{line1} or R_{flt} on the dc fault response for a LCL-VSC are similar as for a L-VSC and are not replicated.

7.2 Simulations of Blocked LCL-VSC under dc fault

Fig. 8 shows the simulation of LCL-VSC with L_{line1}=0.01H and R_{flt}=0.01 Ω. IGBTs of the LCL-VSC are blocked at the same time when the dc fault is applied. In line with the conclusions for a *L*-VSC, simulation results confirm accuracy of *dq* frame AVM LCL VSC diode bridge model.

Comparing Fig. 8 (a), (b) with Fig. 6 (a), (b), we can see that ac fault current of a LCL-VSC is significantly lower than ac current of an L-VSC, which is consistent with conclusions from [15]. However, there is still high dc fault current during the freewheeling stage. As indicated in Fig. 8 (d), dc voltage of the dc capacitor stays at zero during the freewheeling stage, which is consistent with conclusions from [12].



(a) d-channel current (b) q-channel current

(c) dc current (d) dc voltage

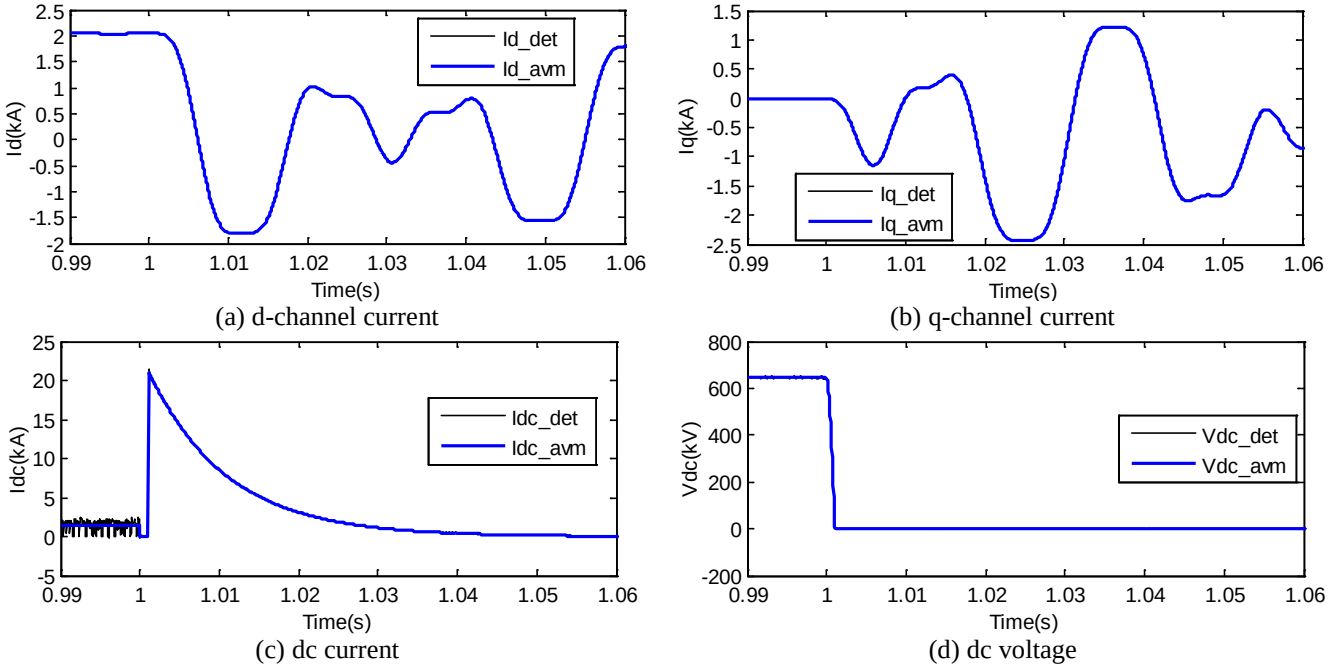
Fig. 8 Simulation of LCL-VSC with R_{flt}= 0.01Ω, L_{line1}=0.01H

7.3 Simulation of controlled LCL-VSC under dc fault

Fig. 9 shows the simulation results of a LCL-VSC which retains full control during dc fault. The controller reduces M_d and M_q to zero during dc fault in order to reduce dc fault current. The dc fault is essentially converted to a three-phase ac fault with zero fault resistance under such circumstances. The curves from AVM are almost the same as the simulation curves from detailed switching model.

Comparing Fig. 9(a) and (b) with Fig. 8 (a) and (b), we can see that dynamics at the ac side are the same and ac current magnitude is low. The ac current is the current through active IGBT switches (2-level VSC) and therefore they need not be blocked.

Fig. 9(c) shows that under the operating condition of M_d=M_q=0 during dc fault, the initial dc current provided by the LCL-VSC is high but reduces to zero after the free-wheeling (through diodes) stage.



(a) d-channel current (b) q-channel current

(c) dc current (d) dc voltage

Fig. 9 Simulation of LCL-VSC with M_d=M_q=0 during dc fault

7.4 Comparison of the simulation speed and simulation step

Table 1 illustrates the simulation speed advantage of using *dq* frame VSC diode bridge model, when compared with ABC frame detailed model. It is expected that the increase of simulation speed will be more significant for a dc system with larger number of VSCs. It has also been tested that the *dq* frame AVM for L-VSC and LCL-VSC is able to achieve accurate simulation results with simulation step increased up to 500μs.

Table 1 Comparison of the simulation speed between ABC and dq frame models

Model	Frame	Simulation time for 1.5s real time using same 10μs simulation step	Allowable maximum time step to achieve accurate results
L-VSC	ABC detailed	7.5s	10 μs
	dq AVM	1.1s	500 μs
LCL-VSC	ABC detailed	4.29	10 μs
	dq AVM	2.18	500 μs

8 MMC Model Verification

8.1 Parameters of the tested MMC

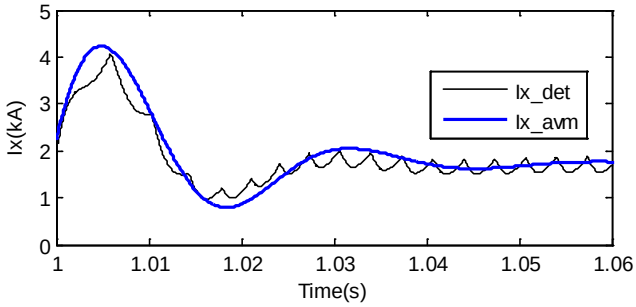
A test MMC is simulated using MMC *dq* frame AVM and MMC ABC frame detailed model. Arm current is 0.044H, submodule capacitance is 0.65mF and number of voltage levels is 21. Parameters for

the ac system and dc system are exactly the same as the LCL-VSC and L-VSC. A permanent pole to pole dc fault is applied at 1.0s and a range of dc fault resistances is tested.

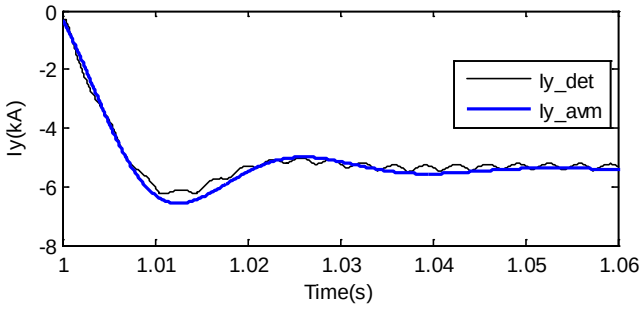
8.2 Simulations of MMC During low residual dc voltage

Fig. 10 compares the blocked MMC dq model with detailed MMC model during dc fault. In this test, R_{flt}=20 Ω and the average steady state residual dc voltage is about 120kV, which is around 20% the rated dc voltage. Fig. 10 shows that the *dq* MMC achieves accurate results as the detailed MMC model in ABC frame.

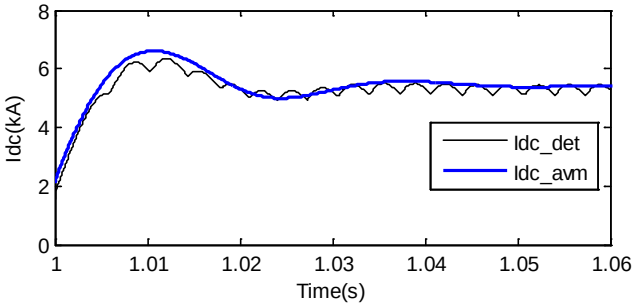
The further tests with higher residual dc voltage demonstrate excellent model accuracy. As residual dc voltage drops below 20%, the accuracy diminishes, but such low dc voltage at dc terminal of MMC is not very likely with practical dc faults because of DC CBs (DC circuit breakers) associated with MMC [13]. As reported in [13], the line side dc voltage of a DC CB drops to zero during dc fault and the bus side dc voltage of a DC CB (dc voltage at dc terminal of a MMC) remains above 35% the rated dc voltage.



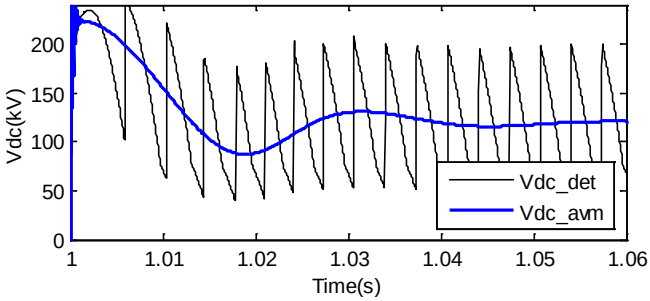
(a) x-axis current



(b) y-axis current



(c) dc current



(d) dc voltage

Fig. 10 Simulation of MMC with R_{flt}= 20Ω, L_{dc}=0.1 H

8.3 Application and disadvantages of the modelling method

The modelling in dq frame has the merit of converting the ac quantities to dc quantities resulting in elimination of 50Hz oscillation which improves the simulation speed. Also dq frame modelling enables

linearization. With the proposed blocked state model, dq modelling can also be used for dc fault condition, but note that two equations are replaced in fault condition while model topology is the same.

The *dq* frame model also has a number of weaknesses, related to accuracy:

- dq frame modelling is normally derived from average model in ABC frame. Representing switching actions and non-linear phenomena in DQ frame is difficult.
- The dq frame modelling cannot be used for harmonic study (unless another dq frame at harmonic frequencies is introduced).
- It is not ideally accurate for blocked MMC in the case when the dc voltage is very low (below 20% of the rated dc voltage). Zero DC voltage is a singularity case, and all the above assumptions will break down.
- The proposed modelling method is not directly applicable during pole-to-ground DC fault, since such fault shorts only half DC capacitance and therefore DC topology changes further.

9 Conclusions

The issue of modelling a VSC as a current source converter during dc fault was confirmed and analysed in depth. A new method of modelling a blocked VSC in a rotating *dq* frame during dc fault is mathematically derived and verified. Based on the new modelling method, a unified dynamic model of VSC for both normal operation and dc-fault response is proposed. Simulation results verified that the proposed model is able to replace the detailed switching model for pole-to-pole dc fault study. The dc fault response of a VSC during the first few milliseconds after dc fault are also well represented, which indicates that the proposed model is adequate for fast modelling of the future large dc grids. It is demonstrated that the proposed model can be applied for fault-tolerant LCL VSCs and for latest MMC converters operating in blocked conditions.

10 Acknowledgments

Financial support from European Research Council in FP7 grant no 259328, 2010 is acknowledged.

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12 Appendix

Table 2 Parameters of the ac system

V_{srx}(kV)	R_s(Ω)	L_s(H)
326.6	2	0.05

Table 3 Parameters of the dc system

$E(kV)$	C_{dc}+C_{line1}(μF)	R_{line1}(Ω)	R_{line2}(Ω)	R_{flt}(Ω)	L_{line1}(H)
±320	24	1	0.8	0.01,10 or 100	0.001, 0.01 or 0.1

Table 4 Parameters of the ac transformer of the tested L-VSC

R_k(Ω)	L_k(H)	k
0	0.0764	1.1364

Table 5 Parameters of the LCL circuit of the test LCL-VSC

R_1(Ω)	L_1(H)	R_2(Ω)	L_2(H)	$C(\mu F)$
0.0273	0.3347	0.0291	0.3565	20.4