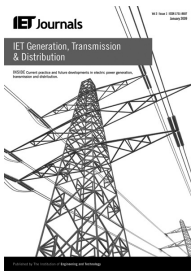
Published in IET Generation, Transmission & Distribution
Received on 15th April 2014
Revised on 16th September 2014
Accepted on 10th October 2014
doi: 10.1049/iet-gtd.2014.0348



ISSN 1751-8687

3-Level cascaded voltage source converters controller with dispatcher droop feedback for direct current transmission grids

Ali Akbar Jamshidifar, Dragan Jovcic

School of Engineering, University of Aberdeen, Aberdeen, AB24 3UE, UK
E-mail: d.jovcic@abdn.ac.uk

Abstract: The future direct current (DC) grids will require additional control functions on voltage source converters (VSC) in order to ensure stability and integrity of DC grids under wide range of disturbances. This study proposes a 3-level cascaded control topology for all the VSC and DC/DC converters in DC grids. The inner control level regulates local current which prevents converter overload. The middle control level uses fast proportional integral feedback control of local DC voltage on each terminal which is essential for the grid stability. The hard limits (suggested ±5%) on voltage reference will ensure that DC voltage at all terminals is kept within narrow band under all contingencies. At the highest level, each station follows power reference which is received from the dispatcher. It is proposed to locate voltage droop power reference adjustment at a central dispatcher, to maintain average DC voltage in the grid and to ensure optimal power flow in the grid. This slow control function has minimal impact on stability. Performance of the proposed control is tested on PSCAD/EMTDC model of the CIGRE B4 DC grid test system. A number of severe outages are simulated and both steady-state variables and transient responses are observed and compared against conventional droop control method. The comparison verifies superior performance of the proposed control topology.

1 Introduction

High voltage direct current (HVDC) transmission based on voltage source converters (VSC) has become accepted technology in many projects worldwide. Although used solely for point-to-point transmission, there has been significant interest for developing HVDC grids [1–4].

Although HVDC VSC converter control is well established in industry, the VSC converter control in DC grids will be different. A converter will be required to respond to DC grid disturbances in order to ensure stability and integrity of the whole DC grid.

DC voltage droop feedback control method has been extensively studied for DC grids and in general for parallel connected converters like in micro grids [5–10]. This is a very good approach since local power order at each converter is moderated in response to DC grid situation which is detected through DC voltage variation. The method is also robust, since only local feedback signals are used for control at each terminal and no grid-wide communication is required. This method resembles the widely used frequency droop feedback with generators in AC systems.

However this approach has several principal disadvantages:

- Unlike frequency in AC systems, DC voltage is different at each point in DC grid and furthermore it changes with variation in operating conditions. Therefore it is difficult to determine DC voltage references for each terminal at each operating scenario.
- The droop gain values also will have impact on transient performance and small-signal stability. Large droop gains are desired to keep DC voltage within narrow range (in steady-state), but generally large droop gains deteriorate small signal stability.
- In case of extreme contingencies (loss of one or more major terminals), the DC voltage deviations may be large, considering that droop feedback is essentially proportional control which is unable to completely eliminate error.
- One converter is normally in DC voltage control mode (slack bus) with integral control action. If this terminal is lost the DC voltages deviates considerably from their nominal values which may damage the components or the grid may not operate in optimal condition. A communication from dispatcher is required to allocate another station to control DC voltage.

The use of adaptive droop [11] may improve responses in different operating conditions but other issues will remain.

Barker and Whitehouse [12] proposes considerably different approach where load reference set point (LRSP) is used with inner DC voltage control at each terminal. The significant advantage of this method is the use of DC voltage control and also the use of identical control topology at each DC grid terminal. This 2-level control method still uses fast droop feedback (V_{DC}-I_{DC}) at each

terminal and may not be able to achieve exact power flow unless LRSP signals are timely adjusted at each terminal.

In this article we aim at developing terminal-located control to enable very robust DC grid operation. The highest emphasis of this VSC terminal-based control is placed on grid stability, transient response, tight DC voltage control and independent operation of terminals.

We will also develop another, much slower controller which deals with long-term power balance and optimal grid power flow. We will therefore try to separate fast grid stability controls from long-term optimal power dispatch.

Although in most references only steady-state power flow is studied, we believe that DC grid control methods should be confirmed for both: post fault power flow (steady state values for all variables) and fast transient responses (dynamic stability). We will use detailed model of the recently proposed CIGRE (B4.57 and B4.58) DC grid test system [13] and evaluate performance for a range of most serious outages.

2 DC grid control strategies

2.1 DC voltage control in DC grids

DC voltage in DC grids plays similar role as frequency in AC systems. It is an indicator of the health of the DC grid. VSC converters cannot operate with low DC voltage (typically below 0.8–0.9 pu) since diodes would conduct uncontrollably. High DC voltage is strictly prohibited because of insulation limits.

However, as power flow in a DC Grid changes, different buses will have different DC voltage values. This significantly complicates development of DC voltage controller and development of any power balancing control method.

The dynamics of DC voltage are much faster than frequency deviations in electro-mechanical AC systems, and time constants can be even below 10 ms. This is the result of fast converter controls, lack of mechanical inertia and lack of reactive component in DC cable impedances. These conclusions call for development of a wide bandwidth and robust DC voltage controller at each VSC terminal.

2.2 Conventional Droop control at VSC converters

The DC voltage droop control at VSC converters is a standard method to provide sharing of power balancing among all terminals. This method is primarily developed using static curves (P-V, I-V) [11, 12] which indicate DC voltage deviations for loading conditions and vice versa.

Fig. 1 illustrates the complete schematic of the VSC converter with DC voltage droop control method. The inner control loops use standard PI controllers with decoupling loops to control the converter current in *dq* frame. The outer control loops regulate active power flow and/or DC voltage on *d*-axis and reactive power flow or AC voltage on *q*-axis. In each DC grid, one terminal will control DC voltage (known as a DC voltage control terminal or slack bus) [13] and the others will regulate active power flow (power control terminals considering the influence of DC voltage droop on P_{DCref}), and they will have DC voltage droop feedback (shown as K_{DCdroop} gain).

2.3 3-Level cascaded control (3LCC) at VSC terminals

Cascade control is a well-known control technique in process industries which splits the control problem in two or more nested control loops [14]. It improves dynamic performance by controlling the intermediate variables and providing limits on their reference values. It also enables zero error tracking of variables at each level assuming integral controls are employed and no saturation.

We are proposing to use cascaded control structure to achieve zero error fast tracking of DC voltage at each terminal. Cascaded control enables automatic adjustment of DC voltage reference according to power flow conditions. We will remove power-droop function from the terminals, since fast control of DC voltage will provide grid stabilisation.

Fig. 2 illustrates the outer and middle control loops of the proposed 3LCC strategy for the *d*-axis of onshore VSCs. The inner current control loops are same as droop control of Fig. 1.

The three control loops of the proposed 3LCC are

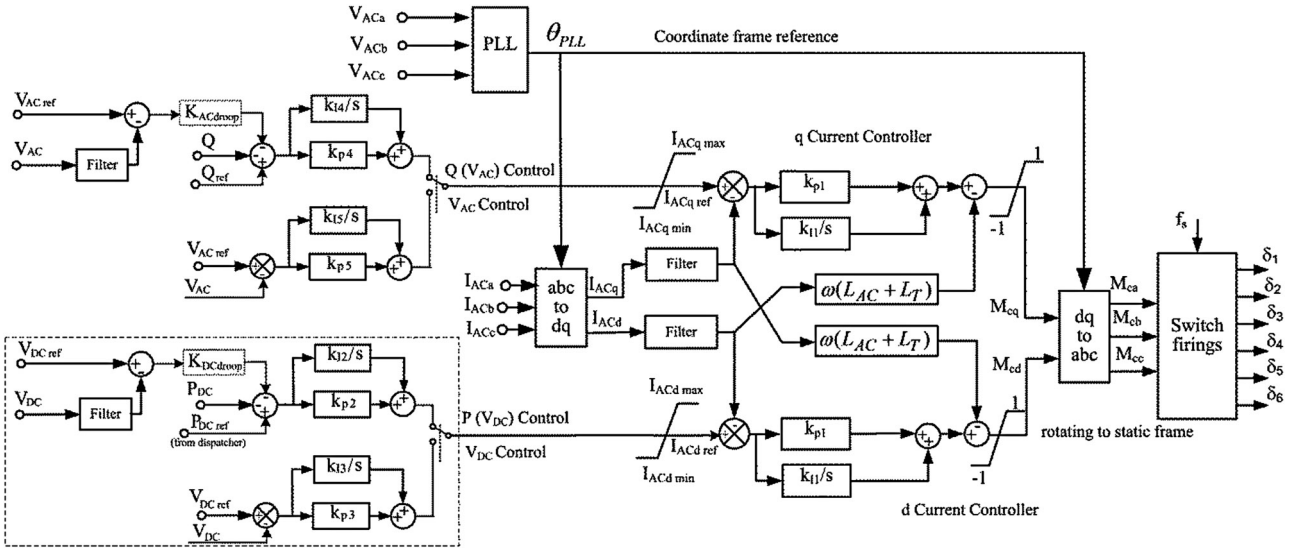


Fig. 1 *Schematic of the VSC controller with typical droop DC voltage feedback*

IET Gener. Transm. Distrib., pp. 1–9
doi: 10.1049/iet-gtd.2014.0348

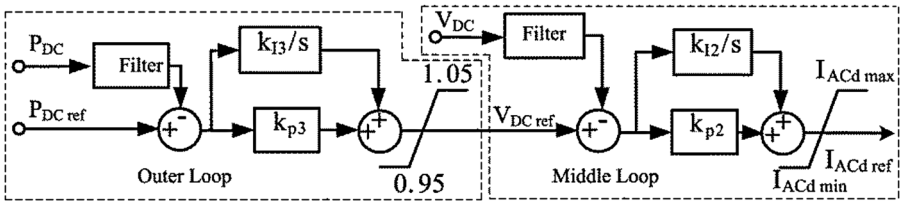


Fig. 2 *Proposed control structure of 3LCC for d-axis of VSCs*

- The inner PI control loop which is shown in Fig. 1. It has the highest bandwidth to be able to fast track the converter currents. The reference values are limited according to converter ratings. If the current reference hits the limit ($I_{ACdref} = I_{ACdmax}$) then the converter is in saturation at full power. This implies that it is not possible to regulate variables at higher control levels (DC voltage and power). In such situation terminal sends 'current-limit alert' message to the dispatcher.
- The middle loop PI controller at each station is designed to regulate the local DC voltage. It is proposed to use proportional-integral control action to enable exact tracking of DC voltage at each terminal, while gain values can optimised to avoid underdamped transients or instabilities. The reference DC voltage V_{DCref} is provided from the third level power controller and each terminal will have different DC voltage reference. There is a ±5% hard limit on V_{DCref}, $[0.95 < V_{DCref} < 1.05]$, since V_{DC} should not be allowed to stay outside this range at any of the DC grid terminals. This limit guaranties that the steady-state DC voltage stays within the desired range. V_{DCref} will hit a limit in case that reference power cannot be achieved. In such situation terminal would send 'DC voltage-limit alert' message to the dispatcher. The use of ±5% hard limits and integral control on V_{DC} ensures high priority for V_{DC} control at each terminal. The power control is only enabled if the terminal voltage is within ±5%.
- The outer level provides power control according to reference and local power measurement. Each terminal receives power reference from the dispatcher. This controller is also of PI type to enable exact power reference tracking with good transients but it is set to be slower since it has no importance for system stability. Normally power references from dispatcher will be accurate.

Located at the highest level is a dispatcher controller which is common for a dc grid.

In a short time interval after a major outage (component tripping) we assume that dispatcher is inactive and therefore it will not be possible to change power reference at terminals. One of the converters will hit the ±5% voltage limit and it operates as a slack bus. If additionally this converter hits current rating limit before new power balance is achieved, then control is lost and DC voltage at that terminal moves outside ±5% limits. Then the next terminal hits ±5% voltage limit and automatically becomes next slack bus. This process continues until a new power balance is achieved. It is evident that transition from one to another slack bus is achieved inherently (no need for dispatcher action) enabling very robust, reliable grid response.

The actual ±5% limit is suggested since the steady-state DC voltages beyond this band are not usually allowed in DC grids. However, the limits can be adjusted independently at each terminal.

2.4 Dispatcher central controller

The role of dispatcher is to send the power references to each terminal corresponding to the actual situation in the whole grid, and to the power trading arrangement. This can be done automatically (large DC grids) or manually (smaller grids) and is assumed to be slow process (time constants of seconds or minutes). Normally, however, dispatcher should be able to adjust power references to follow typical load/generation changes like wind speed changes.

Fig. 3 shows the structure of proposed automatic dispatcher controller. This is DC voltage droop controller, but the time constants are longer than with conventional terminal-located droop. The values for desired powers for each of the n terminals (P_{des1}, P_{desn}) are received from the power trading market and considering merit order dispatch.

The gains d_1, d_2, $\ldots d_n$ moderate the power references at each terminal according to the prevailing grid conditions and their values can be a part of the market agreements. These gains play the role of droop feedback which adjusts terminal power references according to DC grid power balance.

The dispatcher continuously receives DC voltage values from each DC bus (V_{DC1}, $\ldots V_{DCn}$) and calculates average DC voltage for the grid V_{DCav}, which should ideally be 1 pu. If the average DC voltage deviates then all power references are adjusted according to gains d_1, $\ldots$ d_n. The advantage of having droop adjustment at dispatcher centre (rather than at each of the terminals) is that one common DC voltage (the average value) is employed and the reference value is same for all terminals and for all power flow conditions. Also, averaging will eliminate high-frequency dynamics and enable droop control to respond only to global power unbalance, which will have minimal dynamic impact on the grid.

If dispatcher receives 'DC voltage-limit alert' message from a terminal this would imply that power balancing action has been inadequate or slow for that terminal. The appropriate dispatcher action would be to change P_{des} (up or down) for this terminal. If a 'current-limit alert' is received then a larger change in P_{des} is recommended.

2.5 DC/DC converter control

DC/DC converters will be used in DC grids [4] and they are included in the CIGRE B4 DC grid test system in [13]. A

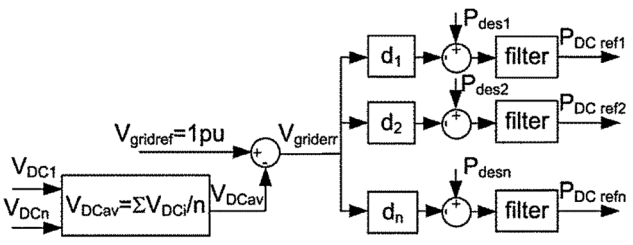


Fig. 3 *Control structure at the dispatcher centre*

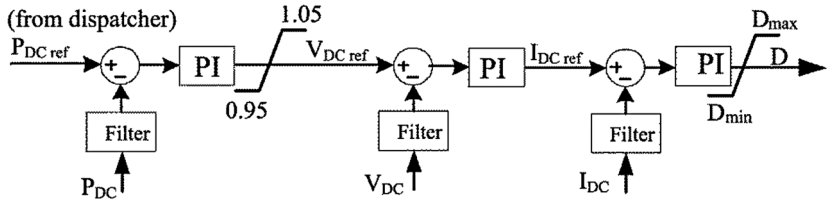


Fig. 4 *Control structure of the DC/DC converters*

similar 3LCC strategy is adopted for DC/DC converters in this study, as shown in Fig. 4. A simple DC chopper is used as the DC/DC topology and the control signal is the duty ratio D.

2.6 Wind farm VSC converter control

The VSC converters connected to wind farms will be controlled to establish offshore AC system frequency and to maintain power balance in the offshore grid [13]. These converters will not be able to respond to DC grid signals and they are seen as constant power sources in the DC grid. The controllers have a two levels topology, where the inner loops are the same as in Fig. 1. The outer control loops regulate the corresponding *dq*-components of the AC voltage as shown in Fig. 5 and in this way the converter balances the power on the offshore island. Note that a DC grid may also have other uncontrollable power converters, depending on the future grid connection standards.

3 CIGRE B4.57, B4.58 DC grid test system

The CIGRE DC grid test system is developed jointly by the two CIGRE working groups (B4.57 and B4.58) to provide common platform for testing DC grid models and control strategies [13]. The main focus of this test system is DC grid and the converter control while the AC sections are considered as simple as possible. Fig. 6 shows the layout of this test system. The following labelling is used for busses and for converters:

Ba: Bus onshore AC (onshore AC bus).
Bo: Bus offshore AC (offshore AC bus).
Bm: Bus Monopole (DC bus at monopole 400 KV system).
Bb: Bus Bipole (DC bus at bipole 800 KV DC system).
Cm: Converter Monopole.
Cb: Converter Bipole.
Cd: DC/DC Converter.

The complete CIGRE DC grid test system is developed in PSCAD. All the controllers are represented in full detail

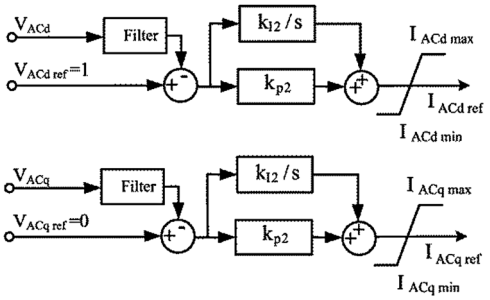


Fig. 5 *Control structure of the wind farm VSC converter*

(including PLL) but VSC converters are represented using average value models. Two different control options are considered for all onshore and DC/DC converters: 3LCC control from Fig. 4 and droop control from Fig. 1, as presented in [13]. The controller gains for the onshore VSCs (*d*-axis) and DC/DC converters of the two control methods are given in Table 1. The gains for inner current control loops are same for both methods and they are designed considering a VSC converter with local AC grid in isolation. The PI gains for the outer loop of DC voltage terminals (Cm-A1, Cb-A1 and Cm-B3) in droop control method are $Kp = 0.5$ and $Ki = 10$. All the input and output variables in the controllers are in pu.

With droop control the outer (power) control gains are designed to enable power reference tracking but the control is sufficiently slow not to interfere with the inner loop dynamics. The droop gain is increased as much as dynamic responses will allow. This gain is also tested for recovery after DC faults and it was necessary to relax the gains (both power control and droop) because of observed dynamic instabilities.

With 3LCC, the middle loop (Vdc control) is designed considering a VSC converter with local AC grid in isolation. The gains are increased as much as possible to enable tight DC voltage control with up to 20% overshoots. Large gains in the middle loop also give good responses following DC faults. The outer (Power) control is very slow while enabling power reference tracking, and the gains are lower than power control with droop methods.

The high values for dispatcher gains ($d_1 = d_2 = \ldots d_n = 10$) are selected to enable good steady-state control of average DC voltage, while the dispatcher filter time constant is 2 s. This low-bandwidth filtering eliminates dynamics from the dispatcher droop feedback which has good impact on dynamics of the DC grid.

4 Steady-state testing

Fig. 6 shows the steady-state power flow data obtained on the 3LCC model (the droop control gives very similar power flow). It is seen that all DC voltages are within ±2% of the rated value and there is no saturation of any DC voltage control loop. In this condition the DC grid operates with all converters in normal power control mode. This will be normal operating condition since it is expected that dispatcher will be sending accurate power references. A large number of different tests are simulated to evaluate the performance of the proposed control:

- Case 1: Outage of DC Cable Bb-A1 – Bb-C2.
- Case 2: Outage of DC-DC Converter Cd-E1.
- Case 3: Outage of DC-DC Converter Cd-B1.
- Case 4: Outage of DC Cable Bm-B2 – Bm-B3.
- Case 5: Outage of Converter Cb-A1.
- Case 6: Outage of OHL Bb-A1 – Bb-B4.

doi: 10.1049/iet-gtd.2014.0348

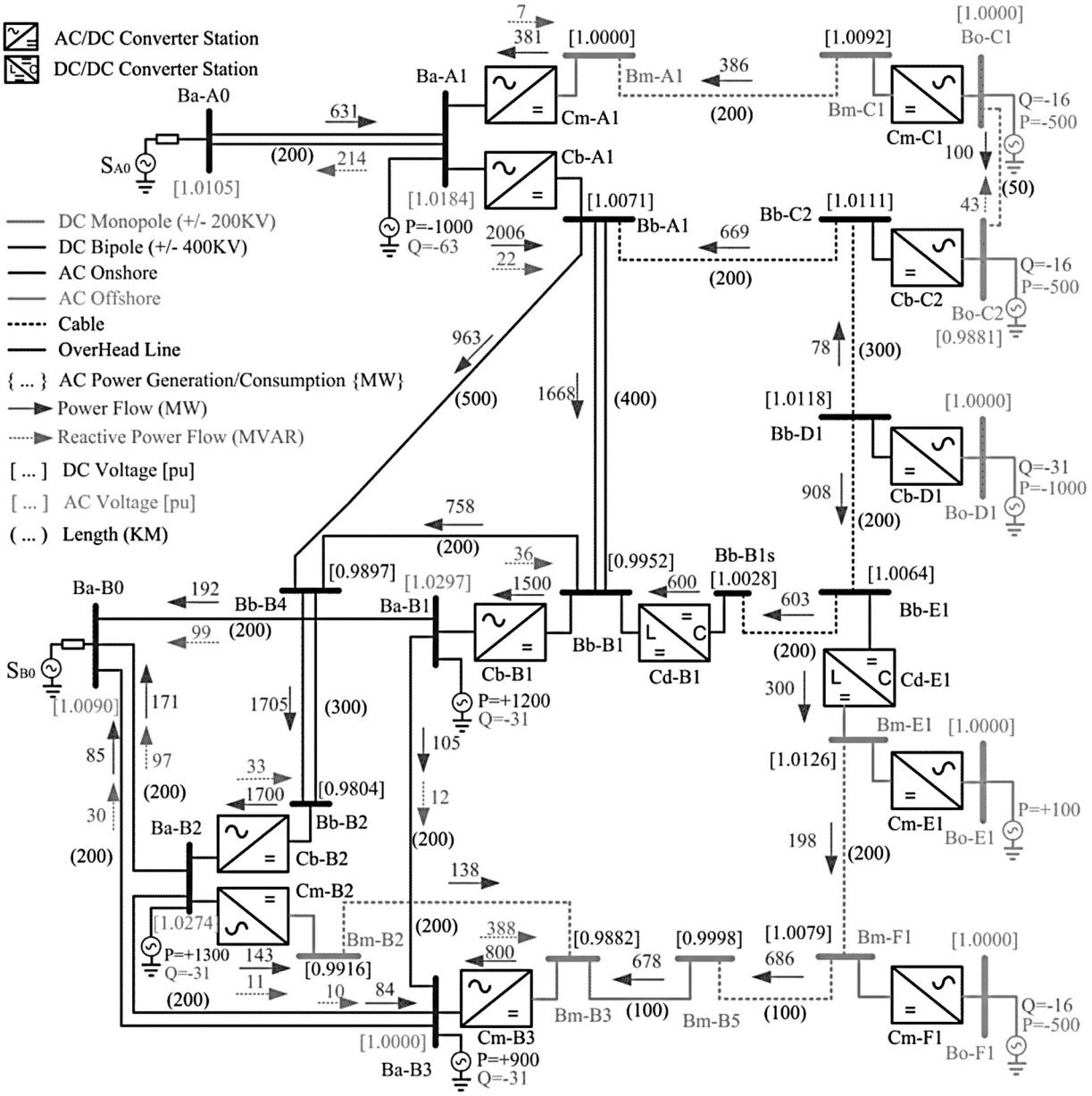


Fig. 6 *CIGRE B4.57 and B4.58 DC grid test system with steady-state power flow*

- Case 7: Outage of Converter Cb-B2.
- Case 8: Outage of OHL Cable Bm-B5 – Bm-B3.
- Case 9: Severe power reference step change on Converter Cm-B3 (−800 to 1200 MW)

The VSC outages are simulated by blocking the converter's and opening the converter's AC circuit breaker. The DC cable/line outages are simulated by applying pole-pole DC fault and opening DC circuit breakers on both cable ends after a specified fault clearance time (5 ms by default). The outages of DC/DC converters are also simulated by opening the DC circuit breakers on both sides after the specified fault clearance time. The power references are kept constant at all terminals. The test case 9 simulates a severe communication fault between the dispatcher and terminal Cm-B3.

Table 2 gives the steady-state DC voltages before and after the 9 test cases for the two control methods. The test system is a large system and some DC nodes are not shown for brevity. The table shows that all post-contingency DC voltages for the

Table 1 The control gains for *d*-axis onshore VSCs and DC/DC converters

Control method	3LCC, pu/pu			Droop control, pu/pu		
	Inner loop Kp, Ki	Middle loop Kp, Ki	Outer loop Kp, Ki	Inner loop Kp, Ki	Outer loop Kp, Ki	Droop gain Kdroop
VSCs	0.5, 10	4, 80	0.5, 1	0.5, 10	1, 20	5
DC/DC	0.05, 1	1, 15	0.5, 1	0.02, 1.5	0.5, 5	5

Table 2 DC voltages (pu) with the two control methods before and after faults

DC bus	Control method	Before fault	After fault								
			Case 1	Case 2	Case 3	Case 4	Case 5	Case 6	Case 7	Case 8	Case 9
Bm-B2	3LCC	0.9916	0.9915	0.9851	0.9915	***1.0500***	0.9866	0.9915	0.9966	0.9506	*1.0439*
	droop	0.9900	**Unstable**	0.9900	0.9900	0.9900	0.9900	0.9900	0.9900	0.9900	**1.0741**
Bm-B3	3LCC	0.9882	0.9881	*0.9788*	0.9882	0.9633	0.9810	0.9881	0.9953	***0.9500***	***1.0500***
	droop	0.9867	**unstable**	0.9804	0.9867	0.9724	0.9869	0.9866	0.9869	0.9721	**1.0924**
Bm-F1	3LCC	1.0079	1.0078	0.9903	1.0078	0.9854	0.9940	1.0078	1.0207	***1.0611***	***1.0561***
	droop	1.0064	**unstable**	0.9918	1.0064	0.9940	1.0064	1.0064	1.0065	**1.1586**	**1.0995**
Bb-A1	3LCC	1.0071	0.9787	*1.0100*	1.0045	1.0065	0.9653	1.0117	*1.0349*	*1.0134*	*1.0115*
	droop	1.0100	**unstable**	1.0100	1.0100	1.0100	**0.9170**	1.0100	1.0100	1.0100	1.0100
Bb-B1	3LCC	0.9952	0.9702	0.9971	0.9892	0.9948	*0.9616*	0.9928	1.0255	0.9994	0.9981
	droop	0.9981	**unstable**	0.9981	0.9950	0.9981	**0.9134**	0.9928	1.0042	0.9981	0.9981
Bb-B2	3LCC	0.9904	0.9539	0.9815	*0.9753*	0.9801	*0.9533*	*0.9710*	1.0281	0.9830	0.9822
	droop	0.9834	**unstable**	0.9834	0.9814	0.9834	**0.9056**	0.9726	1.0058	0.9834	0.9834
Bb-E1	3LCC	1.0064	1.0371	1.0155	1.0163	1.0046	0.9695	1.0110	*1.0316*	*1.0268*	*1.0204*
	droop	1.0093	**unstable**	1.0155	1.0217	1.0081	**0.9196**	1.0082	1.0107	1.0234	1.0180
V_{DCav} DCS2	3LCC	1.0001	1.0000	0.9856	1.0000	0.9934	0.9887	1.0000	1.0107	1.0146	**1.0507**
	droop	0.9985	—	0.9878	0.9985	0.9883	0.9985	0.9985	0.9987	**1.0855**	**1.0915**
V_{DCav} DCS3	3LCC	1.0002	1.0000	1.0043	1.0000	0.9994	0.9646	0.9996	1.0320	1.0093	1.0065
	droop	1.0029	—	1.0049	1.0057	1.0028	**0.9164**	0.9989	1.0095	1.0072	1.0056

3LCC controls are constrained within ±5% of the rated values except the offshore DC voltage at bus Bb-E1 for test case 8 (just above 6%). This is expected since wind farms cannot control DC voltage.

It is seen that the post-contingency DC voltages with the droop control method show higher deviations in many test cases. For example, some DC voltages fall by 10% for test case 5 and overshoot over 15% for test case 8 (bold numbers represent deviations of 5% or more). A larger droop gain can reduce this voltage deviation, but this would lead to unacceptable transient performance.

The last two rows show the average DC voltages for DCS2 & DCS3 subgrids. It is seen that the 3LCC provides DC grid average voltage values closer to 1.0 pu in most cases.

It is also seen that the droop control system is unstable for the test case 1. The system is considered unstable because the DC voltages of busses Bb-C2, Bb_D1, Bb_E1, and Bb_B1s peak over 2.6 pu and some power measurements show steady-state oscillations. The main reason for this instability is the activation of inner current-limit on Cb-A1 which eliminates droop stabilisation at this converter. The authors were able to stabilise this case, but only with very low droop gains which implied significantly reduced performance for many other cases. This current-limit actuation problem does not happen with 3LCC, since middle loop will keep DC voltage within 5% and ignore large power demand from outer power loop.

Table 3 presents the steady-state DC power flows on all the DC lines/cables, while Table 4 gives the power flow at the VSC terminals (both active and reactive power). The 3LCC method generally gives more accurate control of VSC terminal post fault powers.

There is a concern that with 3LCC severe power swings will be seen on just one terminal (that firstly hits the ±5% V_{DC} limit), however power flow tests below show that this does not happen. Only in the cases 4, 8 and 9, one converter hits either 1.05 or 0.95 pu DC voltage limit, while in the other cases no converter hits the DC voltage limit. It is seen that the DC voltage distribution is symmetrical for all cases and the power sharing with 3LCC is better than with droop control method. This improvement happens since dispatcher controller always responds to average DC voltage for all disturbances, while distributed droop has inaccurate local DC voltage references.

Table 3 DC power flows in DC lines/cables (MW) with the two control methods before and after faults

DC line (rating MW)	Control method	Before fault	After fault								
			Case 1	Case 2	Case 3	Case 4	Case 5	Case 6	Case 7	Case 8	Case 9
Bm-B2_Bm-B3 (785)	3LCC	138	139	253	139	0	229	139	55	23	−268
	droop	138	**unstable**	391	139	0	134	139	130	727	−832
Bm-F1_Bm-B5 (785)	3LCC	686	685	391	685	744	448	684	892	0	223
	droop	686	**unstable**	391	686	740	686	686	686	0	272
Bb-A1_Bb-B1 (2 × 2800)	3LCC	1668	1162	1800	2126	1641	515	2630	1368	1965	1871
	droop	1668	**unstable**	1668	2092	1668	457	2397	816	1668	1667
Bb-A1_Bb-B4 (2800)	3LCC	963	818	1029	1092	950	390	0	392	1111	1065
	droop	963	**unstable**	963	1077	963	350	0	234	963	963
Bb-C2_Bb-A1 (1812)	3LCC	669	0	970	1269	608	913	672	538	1346	1133
	droop	669	**unstable**	969	1266	612	815	615	738	1346	1086
Bb-D1_Bb-E1 (1812)	3LCC	908	1567	605	301	969	664	905	1038	222	440
	droop	908	**unstable**	605	303	964	762	962	839	222	488
Bb-B1s_Bb-B1 (2000)	3LCC	600	1245	600	0	600	600	600	515	600	600
(Converter Cd-B1)	droop	600	**unstable**	600	0	600	456	653	533	600	600
Bb-E1_Bm-E1 (1000)	3LCC	300	299	0	299	364	58	298	512	−387	−166
(Converter Cd-E1)	droop	300	**unstable**	0	300	360	300	300	299	−387	−118

doi: 10.1049/iet-gtd.2014.0348

Table 4 Active and reactive power flows of VSCs (MW/MVAR) with the two controls method before and after faults

VSC (rated MW)	Control method	Before fault, MW/MVAr	After fault, MW/MVAr								
			Case 1	Case 2	Case 3	Case 4	Case 5	Case 6	Case 7	Case 8	Case 9
Cb-A1	3LCC	2006/22	2011/21	1909/26	2012/21	2026/21	0/0	2016/21	1243/42	1787/30	1856/28
(2 × 1200)	droop	2006/22	**unstable**	1705/33	1962/24	2063/22	0/0	1832/28	323/32	1328/41	1589/36
Cb-B1	3LCC	−1500/36	−1496/36	−1598/36	−1494/36	−1480/36	−645/12	−1490/36	−2263/25	−1719/35	−1650/35
(2 × 1200)	droop	−1500/36	**unstable**	−1500/36	−1463/36	−1500/36	−485/6	−1437/35	−1574/28	−1500/35	−1500/32
Cb-B2	3LCC	−1700/33	−1695/33	−1798/33	−1694/33	−1680/33	−845/7	−1690/33	0/0	−1919/33	−1850/31
(2 × 1200)	droop	−1700/33	**unstable**	−1700/31	−1676/33	−1700/33	−767/7	−1570/32	0/0	−1700/24	−1700/21
Cm-B2	3LCC	143/11	144/11	259/11	144/11	0/0	234/2	144/11	59/9	27/11	−262/10
(800)	droop	143/11	**unstable**	399/10	134/11	0/0	138/2	143/11	134/−13	747/8	−811/7
Cm-B3	3LCC	−800/388	−799/388	−626/372	−799/388	−718/379	−663/208	−798/388	−927/78	−12/278	55/255
(1200)	droop	−800/388	**unstable**	−763/381	−800/388	−714/379	−801/206	−800/388	−801/83	−712/349	568/89

It is also observed that 'current-limit alert' did not happen in any of the above contingencies.

5 Transient responses

The transient responses are analysed for the above 9 and a range of other contingencies. The monitored performance indicators include stability, overshoot and damping. Only some extreme responses are shown.

5.1 Test case 3 (outage of DC–DC Converter Cd-B1)

Fig. 7 shows the dynamic response of the two control methods for test case 3. It is seen that the DC voltages of bipole buses go up to 1.27 pu with the 3LCC, but they raise up to 1.52 pu with the droop control. Also, several oscillatory modes are excited while damping with 3LCC is consistently better. In case of droop control, the damping of these modes can be improved if droop gains are relaxed, but this generally leads to higher overshoots and wider voltage deviations in steady-state. Note that dispatcher action is not visible in the short time frame in this figure.

5.2 Power reference unbalance

A large power reference unbalance may occur because of failure of one or more communication links with the dispatcher or other issues with central control. This is simulated in case 9 which gives extreme case of 2 GW step difference between the new power references and the actual power flow on CmB3. Fig. 8 shows the transient responses. It is seen that the 3LCC method provides better transient response and steady-state results. The maximum overshoot for 3LCC is 7%, while it is almost 30% for the droop control method. The maximum steady-state offset for 3LCC is <6% while it is 10% with the droop control method.

Many different large power reference disturbance tests were applied to the system. The results verify that the system with 3LCC stays stable for all cases while the droop control system may become unstable for some cases or shows larger DC voltage deviations for other cases.

In case of slow and small disturbances (wind power changes) dispatcher should be able to respond sufficiently fast by sending updated power references. If dispatcher fails to respond to such disturbance, then all DC voltages slide up or down until the converter with extreme voltage hits ±5% limit and then this converter balances the grid power. This scenario is not presented for lack of space and since it

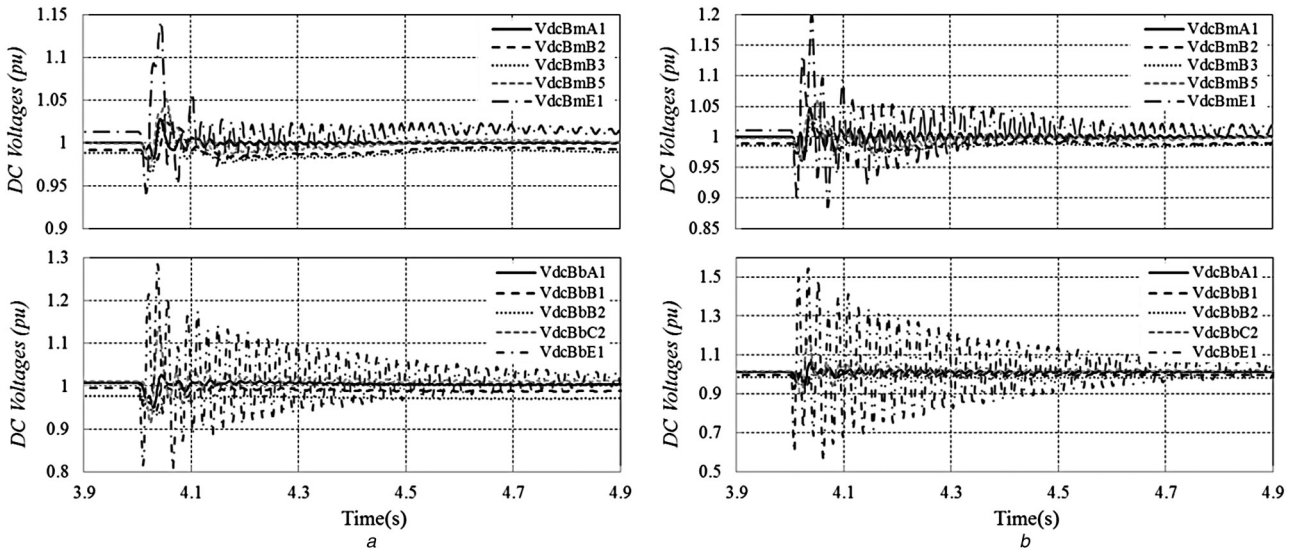


Fig. 7 *DC voltages for test case 3 (Outage of DC-DC Converter Cd-B1)*

a 3LCC control
b Conventional droop control

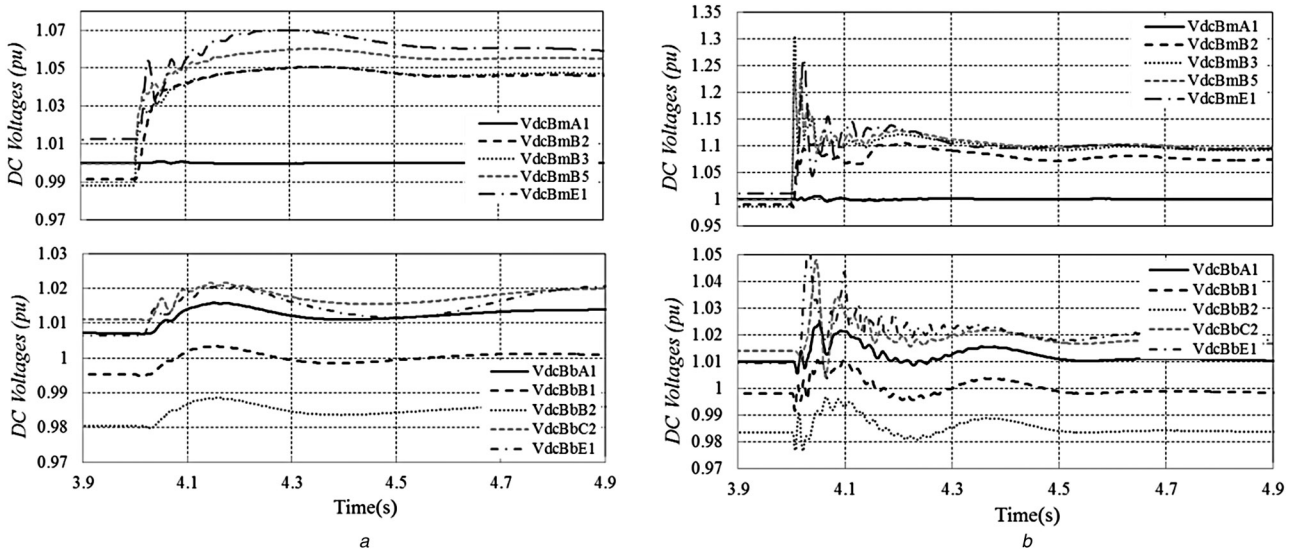


Fig. 8 *DC voltages for test case 9 (reference step change on Converter Cm-B3 (−800 MW to 1200 MW)*

a 3LCC control
b Conventional droop control

is less challenging and gives similar responses as the tests shown.

5.3 Effect of fault clearance time

It is desired to clear the DC faults as fast as possible to prevent overheating/overrating of semi-conductors. However, the DC grid protection systems may require communication between terminals and this entails delays in the fault clearing.

In all previous cases the fault clearance time $t_f = 5$ ms is used. Fig. 9 compares the transient responses for a DC OHL Bb-A1 – Bb-B4 fault (case 6), with 5 ms and 55 ms clearance time. It is evident that with longer clearance times, in particular over 10–20 ms the stability and transient responses deteriorate.

Table 5 shows the maximum clearance time that the grid can tolerate with each of the control methods. The clearance time is gradually increased for each case and the critical time is recorded when stable recovery is impossible. It is seen that the system with 3LCC can tolerate DC fault for slightly longer times. Although the DC faults should be generally cleared within 10–20 ms, it is possible that the faults may remain longer because of failures in protection

Table 5 Critical fault clearance time (ms)

	Case 1	Case 2	Case 3	Case 4	Case 6	Case 8
3LCC	55	>1000	60	60	60	160
droop	Unstable	>1000	55	55	30	160

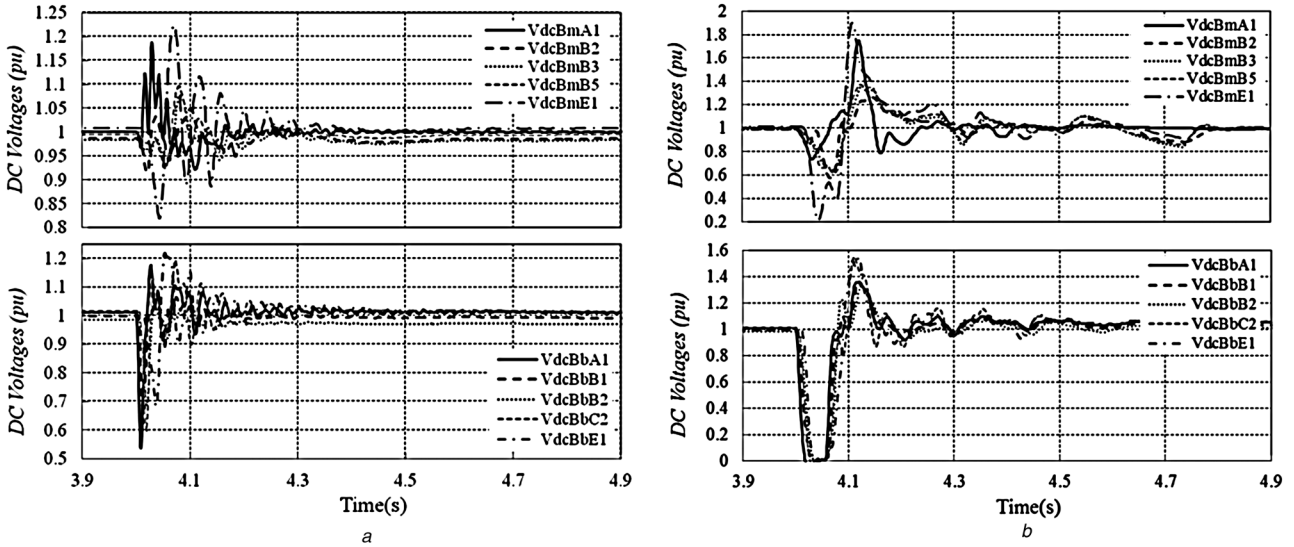


Fig. 9 *DC voltages for test case 6 with 3LCC control (Outage of OHL Bb-A1 – Bb-B4)*

a Clearance time is $t_f = 5$ ms
b Clearance time is $t_f = 55$ ms

doi: 10.1049/iet-gtd.2014.0348

logic or components. In this case the 3LCC provides better reliability for the system.

6 Conclusion

A 3-Level control topology for the VSC and DC/DC converters is proposed as the generic VSC control in DC grids. The fast proportional integral based DC voltage control at each terminal is the essence of this approach enabling excellent stability and tight DC voltage control at all terminals. Since ±5% hard DC voltage reference limits are used, the voltage at all terminals will always stay within this band. The power control is also achieved locally at each terminal, but only if the DC voltage is within the allowed range.

The power reference drooping against average DC voltage variations is located at a central dispatcher since this control is not important for grid stability and only slow changes are required.

The proposed control strategy is implemented on the CIGRE B4 DC grid test system in PSCAD/EMTDC environment. The testing for a range of severe outages demonstrates better stability and DC voltage control when compared with the common droop control. The steady-state power and voltage control is also better with the proposed logic since the dispatcher droop controller responds to average DC voltage for the whole DC grid.

7 Acknowledgment

This project was funded by European Research Council under the Ideas program in FP7; grant no 259328, 2010.

8 References

1 Van Hertem, D., Ghandhari, M.: 'Multi-terminal VSC HVDC for the European Supergrid: obstacles', *Renew. Sustain. Energy Rev.*, 2010, **14**, (9), pp. 3156–3163
2 Jovcic, D., Linden, K., Van Hartem, D., Taisne, J.P.: 'Feasibility of DC transmission Networks'. ISGT Europe, 2011, pp. 1–8
3 Barsali, S., Salvati, R., Zaottini, R.: 'Use of HVDC links for power system restoration', *Electr. Power Syst. Res.*, 2009, **79**, (6), pp. 973–983
4 CIGRE WG B4.52: 'HVDC Grid feasibility study', CIGRE brochure 533, 2013
5 Piagi, P., Lasseter, R.H.: 'Autonomous control of microgrids'. Proc. Power Engineering Society General Meeting, 2006, pp. 496–503
6 De Brabandere, K., Bolsens, B., Van den Keybus, J., Woyte, A., Driesen, J., Belmans, R.: 'A voltage and frequency droop control method for parallel inverters', *IEEE Trans. Power Electron.*, 2007, **22**, (4), pp. 1107–1115
7 Mohd, A., Ortjohann, E., Morton, D., Omari, O.: 'Review of control techniques for inverters parallel operation', *Electr. Power Syst. Res.*, 2010, **80**, (12), pp. 1477–1487
8 Planas, E., Gil-de-Muro, A., Andreu, J., Kortabarria, I., De Alegría, I.M.: 'General aspects, hierarchical controls and droop methods in microgrids: A review', *Renew. Sustain. Energy Rev.*, 2013, **17**, pp. 147–159
9 Majumder, R., Chaudhuri, B., Ghosh, A., Majumder, R., Ledwich, G., Zare, F.: 'Improvement of stability and load sharing in an autonomous microgrid using supplementary droop control loop', *IEEE Trans. Power Syst.*, 2010, **25**, (2), pp. 796–808
10 Haileselassie, T.M., Uhlen, K.: 'Impact of DC line voltage drops on power flow of MTDC using droop control', *IEEE Trans. Power Syst.*, 2012, **27**, (3), pp. 1441–1449
11 Chaudhuri, N.R., Chaudhuri, B.: 'Adaptive droop control for effective power sharing in multi-terminal DC (MTDC) grids', *IEEE Trans. Power Syst.*, 2013, **28**, (1), pp. 21–29
12 Barker, C.D., Whitehouse, R.: 'Autonomous converter control in a multi-terminal HVDC system'. Proc. IET int. Conf. AC and DC Power Transmission, 2010, pp. 1–5
13 Vrana, T.K., Yang, Y., Jovcic, D., Dennetière, S., Jardini, J., Saad, H.: 'The CIGRE B4 DC grid test system'. ELECTRA issue 270, 2013, pp. 10–19
14 Seborg, D.E., Edgar, T.F., Mellichamp, D.A.: 'Process dynamics and control' (John Wiley & Sons, 2010, 3rd edn.)