Analysis of Bidirectional 15MW Current Source DC/DC Converter for Series-Connected Superconducting-Based 1GW/100kV Offshore Wind Farm

Peng Li, Dragan Jovcic, Eoin Hodge, and John Fitzgerald

Abstract—A wind farm with series dc collection can potentially eliminate the costly offshore platform and its step-up components. Multiple series strings can be connected in parallel to extend the power capacity for a given voltage. In such arrangement, the dc/dc converters for individual generators are rated at only a fraction of the transmission voltage. The maturity of superconducting cable technology will eliminate the difficulty of transmission losses with high current low voltage systems. This paper presents a feasibility study on the dc/dc converter design for a parallel-series-connected wind farm. The isolated front-to-front (F2F) mixed voltage source converter (VSC) and current source converter (CSC) is examined with power back-feeding capability during wind calm periods for a 15MW generator. A novel configuration using 3-level (3L) VSC and thyristor-based CSC with combinational control of ac voltage magnitude, frequency, and thyristor delay angle is proposed and evaluated for a 1GW/100kV parallel/series wind farm based on the superconducting cable. Detailed converter model including power loss estimation in PSCAD is presented to support the converter design recommendations.

Index Terms—Offshore wind farm; series dc collection; high-voltage dc (HVDC) transmission; superconducting cable; medium frequency high power dc/dc converter; voltage source converter (VSC); current source converter (CSC); bidirectional power flow.

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I. INTRODUCTION

INCREASED interest in the integration of large scale offshore wind energy using high-voltage dc (HVDC) technologies has been observed due to the long transmission distance [1], [2]. The presently used ac collection method requires an offshore platform to support the step-up transformers, central ac/dc converter, and other ancillaries, which consists of a significant share of the total cost. If dc collection systems are adopted, it might be possible to use a single dc/dc converter stage from the generator output to the HVDC transmission link; thus, the costly offshore platform can be eliminated [3], [4].

Most of the studies on dc collection systems are focused on parallel-connected solutions, either single-stage or multi-stage, which connect to the common HVDC transmission bus [5], [6]. In such systems, each generator converter operates at an optimal current depending on its available wind power. Nevertheless, a parallel-connected dc wind farm also has drawbacks, e.g., dc/dc converter at each wind generator should be rated for full transmission voltage but very low current level, requiring a large number of power semiconductor switches.

Series-connected dc wind farms have been discussed to less extent [7]–[10], but their key advantages are generally known as:

- significantly smaller and less expensive dc/dc converters (including the internal transformers).
- better dc fault handling capability because of inherently controlled dc inductor current.

The primary concerns with series-connected wind farms are the current-source converter design, efficiency, and operating flexibility. First, series connection implies that the transmission cables and generator converters all operate at a higher current than the parallel system. This further complicates the design of current-source dc-dc converter that is significantly constrained by the available semiconductors and the operating frequency. Also, the insulation coordination of series-connected wind farm requires in-depth study due to the uneven voltage stress for the transformers and converter valves. Another challenge lies in the regulation of voltage instead of current for power flow control, such that oversizing of the generator converters with associated control strategies has been suggested [8].

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In a generic matrix-connected (series and parallel) dc wind farm, each string voltage must be shared by individual turbine converters in a way proportional to their power [3], [4], [8]. The comparative studies on the costs and losses are performed in [11]–[13] to offer insights into the various offshore wind dc collection systems, and conclude feasibility and attractiveness of the series-parallel solution.

Various implementations of the series-connected wind farm have been presented in literatures. Since the medium frequency isolation is preferred for safety reasons, it is probably the best solution to add an isolating dc/dc stage following the generator interfacing ac/dc converter and arranged in series at the outputs. [14], [15] present the design of dc/dc converters for 1MW wind generators, using modular topology of single-phase single active bridge dc/dc cells with 1.2kHz medium frequency transformer (MFT). However, their up-scaling for large wind generators beyond 10MW will need high number of cells and potentially large space. Also, in most references of series wind farm, diode bridge is used in the series-connected side, which restricts the power flow in one direction. As a result, diesel generators are necessary to supply the ancillaries, causing increased operating cost and discounted environmental benefit of wind energy. For a series-connected wind farm, bidirectional power flow for individual generator is achieved if the dc/dc converter is able to reverse its dc voltage in the series string, which suggests that CSC bridge should be used. It is further concluded that most existing studies consider relatively small wind farm in a single string of series-connected generators [15], [16].

This study aims for a large offshore wind farm rated at least 1GW with multiple series strings. The initial assumption will be an 1GW/100kV wind farm using parallel-series-connected 15MW generators without offshore platform. A relatively low transmission voltage is allowed by assuming superconducting cables, which offers lower insulation effort but requires high current for the dc/dc converters. The focus of this paper is the design aspects of galvanically-isolated bidirectional dc/dc converters for use in series-connected wind farm. For simplicity, standard generator interfacing ac/dc converters are retained. Then, the bidirectional isolated dc/dc converters using the front-to-front (F2F) mixed VSC and CSC bridges will be evaluated around the issues of their operation, performance, losses, and insulation.

The remainder of this paper is organized as follows: section II states the key initial assumptions and the consequent system configuration with individual dc/dc converter rating; section III discusses the different implementations of the proposed dc/dc converter with PSCAD simulation studies for demonstration; then, a high-level comparison between the series and parallel dc/dc proposals for platform-less wind energy dc collection are presented in section IV; in addition, the associated system level control strategy for series wind farm is analyzed in section V; key conclusions are drawn finally in section VI.

II. INITIAL ASSUMPTIONS AND CONSTRAINTS

A. Superconducting cables

Superconducting dc cables have been intensively developed over the past decades, and the transmission of bulky power is possible with the existing technologies [17]. For long distance applications, the environmental benefit of the superconducting cable system is evident with compact installation and only 10% of ohmic losses of a conventional cable regardless of the voltage level [17]. Recently, a 320kV/10kA superconducting cable has been demonstrated in the EU Best Paths project [18]; and the technology is now close to commercial deployment. The use of superconducting cable is particularly beneficial for the offshore platform-less dc wind farms with single dc/dc stage mainly for two reasons:

1. The dc transmission voltage can be lower (100kV will be assumed in this study). This is significant advantage since the dc/dc converters are installed inside the towers where insulation space is limited. Simplified insulation opens the possibility for single-state conversion, and this enables elimination of offshore platform. Moreover, the lower voltage means a better utilization of the semiconductors.

2. High dc current can be transmitted at low losses, (10kA will be assumed in this study). This eliminates the important disadvantages of series connection, since CSC strings can operate at higher current for better control flexibility.

A major challenge with low transmission voltage is high current, which also manifests in the offshore collection system. Therefore, converters on individual generators will have high current and this implies

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difficulties in selecting suitable semiconductors. The phase-controlled thyristor may be preferred since the alternative is symmetrical self-commutated switches (thyristor type or transistor with reverse-blocking diode) which have less power rating and incur higher losses. As an alternative to high-current converters, a large number of parallel arrays can be introduced, but this implies control difficulties since all arrays would share the same voltage level (but not the same power). Dealing with uneven power generation of individual machines is a generic problem with series connection which becomes more challenging as the number of arrays increases. Also, series connection generally entails higher inter-array cable losses than using parallel connected wind farm and therefore dc-dc converter losses will play important role in the final topology selection.
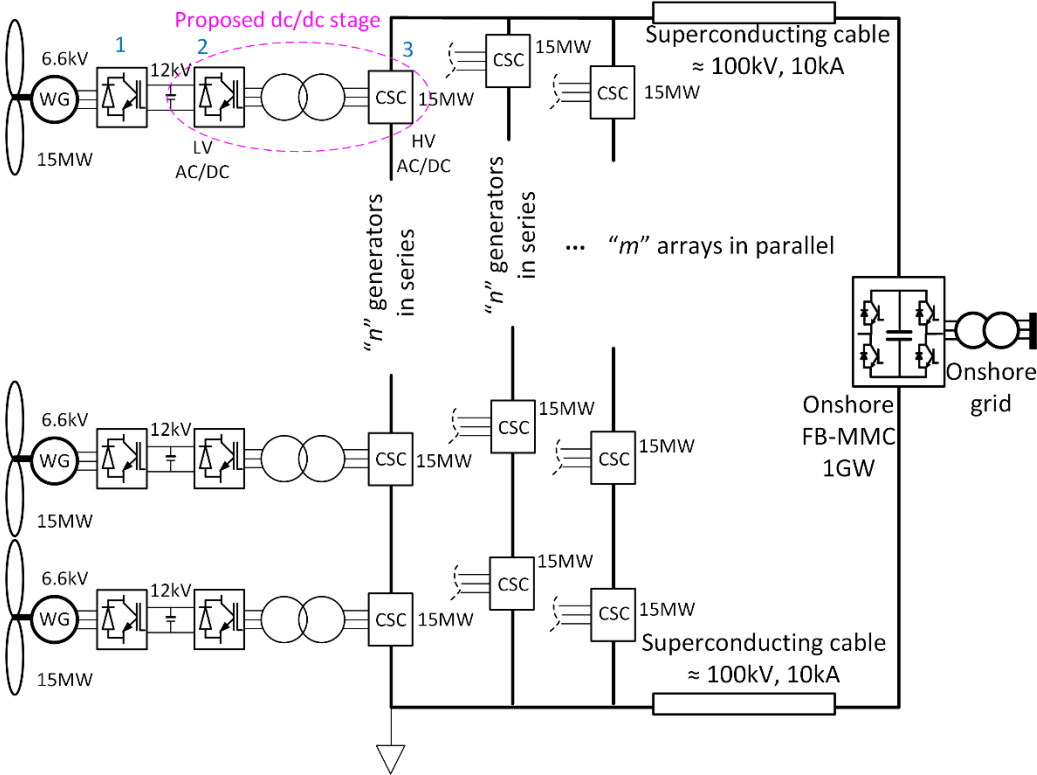
B. Wind farm topology

Fig. 1. System configuration of a 100kV/1GW series-connected offshore wind farm with 15MW generators and superconducting HVDC transmission.

Fig. 1 illustrates the monopole 1GW/100kV parallel-series-connected wind farm studied in this paper, and it can be easily extended into a bipole system with doubled power. The full-bridge (FB) modular

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multilevel converter (MMC) is employed onshore due to its intrinsic dc voltage controllability to benefit the system wide regulation and dc fault protection [19]. In the recent Ultranet HVDC project in Germany, FB-MMC is commercially employed, and the increased losses and cost can be justified by enhanced overall performance [20].

The following assumptions will be adopted in the following discussions:

- Wind farm will have no offshore platforms, and single stage dc/dc converters can fit into the towers.

- Each wind generator should be individually controlled for best power capture.

- For a given wind farm specification, minimized number of parallel generator arrays (m in Fig. 1) will be aimed. The array voltage is the sum of each generator converter voltage in series, which can be variable and unequal for operating flexibility with uneven power generation. This implies that current in each array should be maximized, which brings challenges in selecting the power switches.

- Only bidirectional power options with galvanic isolation will be studied (the diode bridge solution is excluded).

- The fundamental power frequency in the dc/dc converter should be maximized to reduce transformer size. It will be selected in the range 200Hz-500Hz depending on the adopted power switches and operating strategies.

- Type 4 wind generator of 15MW will be employed, with 12kV dc output at 6.6kV generator output voltage [21], [22]. Therefore, bridges 1 and 2 in Fig. 1 will be similar as in conventional type 4 ac grid connected generator; however, bridge 3 needs to be specially designed CSC.

III. DC/DC TOPOLOGIES FOR SERIES CONNECTION

In the proposed dc/dc stage of Fig. 1, its generator facing VSC bridge is termed the low voltage (LV) side; while the CSC bridge in the series array is called the high voltage (HV) side, although its dc voltage can be lower.

In the following discussions, the LV side VSC will assume the 2-level (2L) topology unless otherwise stated [22]; and in this study, its valves will contain 5 series-connected 4.5kV/2kA insulated-gate-bipolar-transistor (IGBT) 5SNA 2000K452300 from ABB to achieve the 12kV/15MW capacity. The HV side CSC (bridge 3 in Fig. 1) can be built by different semiconductor switches, e.g., the phase-controlled thyristor, symmetrical gate-turn-off or gate-commutated thyristor (SGTO or SGCT), or IGBT plus series revers-blocking (RB) diode. Considering the experience with the line-commutated and early generation of VSC-HVDC, the construction of 15MW semiconductor bridge (non-modular) using series-connection of switches is viable, while the 15MW MFT will require development and demonstration to resolve the challenges of higher power frequency, material, losses, and insulation.

A. DC/DC with thyristor-based CSC

The proven CSC technology for high power applications is based on thyristors due to highest current capability, their robustness and low losses. A suitable thyristor would be the Infineon 2.2kV/4.3kA phase-controlled thyristor T4771N with high current capacity, and the resultant wind farm at 930MW/108kV will include two parallel arrays of 31 series generators (i.e., $m=2$, $n=31$ for Fig. 1). Then, each dc/dc converter produces 3.49kV/4.3kA at the rated power of 15MW. The use of high-power generators and high current capacity can reduce the inter-array cabling effort.

The detailed dc/dc configuration is given in Fig. 2. The VSC bridge operates in square wave mode, which implies 120° non-zero level of its phase-to-phase voltage as in Fig. 3(a). The rising edge of such voltage is used as the reference for the CSC thyristor delay angle α, so α has a theoretical limit equal to 120° and serves as the only control degree of freedom. At $\alpha=60°$, the CSC side produces zero dc side voltage and power. Notice that the VSC will not adopt any control on its voltage magnitude to maintain a stable ac voltage reference for the safe commutation of the thyristor-bridge, and the commutation overlap T_u can be calculated by (1), where $I_{dc.cs}$ and $V_{dc.vs}$ are the CSC dc current and VSC dc voltage, L_c is the commutating inductance (i.e. transformer leakage inductance) on the CSC side, and N_t is the transformer step ratio. Then, the CSC

dc output voltage $V_{dc.cs}$ depending on the delay angle α and commutation overlap T_u is expressed in (2) with f_o being the fundamental frequency.

$$T_u = \frac{2L_c \cdot I_{dc.cs}}{N_t \cdot V_{dc.vs}} \tag{1}$$

$$V_{dc.cs} = N_t \cdot V_{dc.vs} \cdot \left(1 - \frac{\alpha}{60°}\right) - \frac{1}{2} N_t \cdot V_{dc.vs} \cdot 6T_\mu \cdot f_o \tag{2}$$
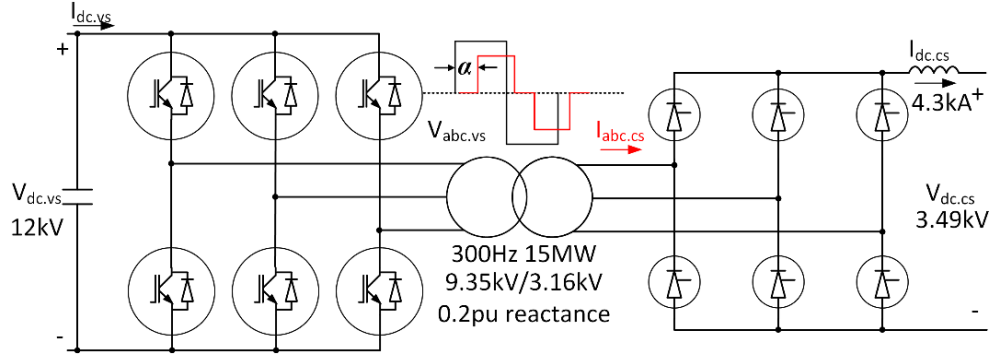

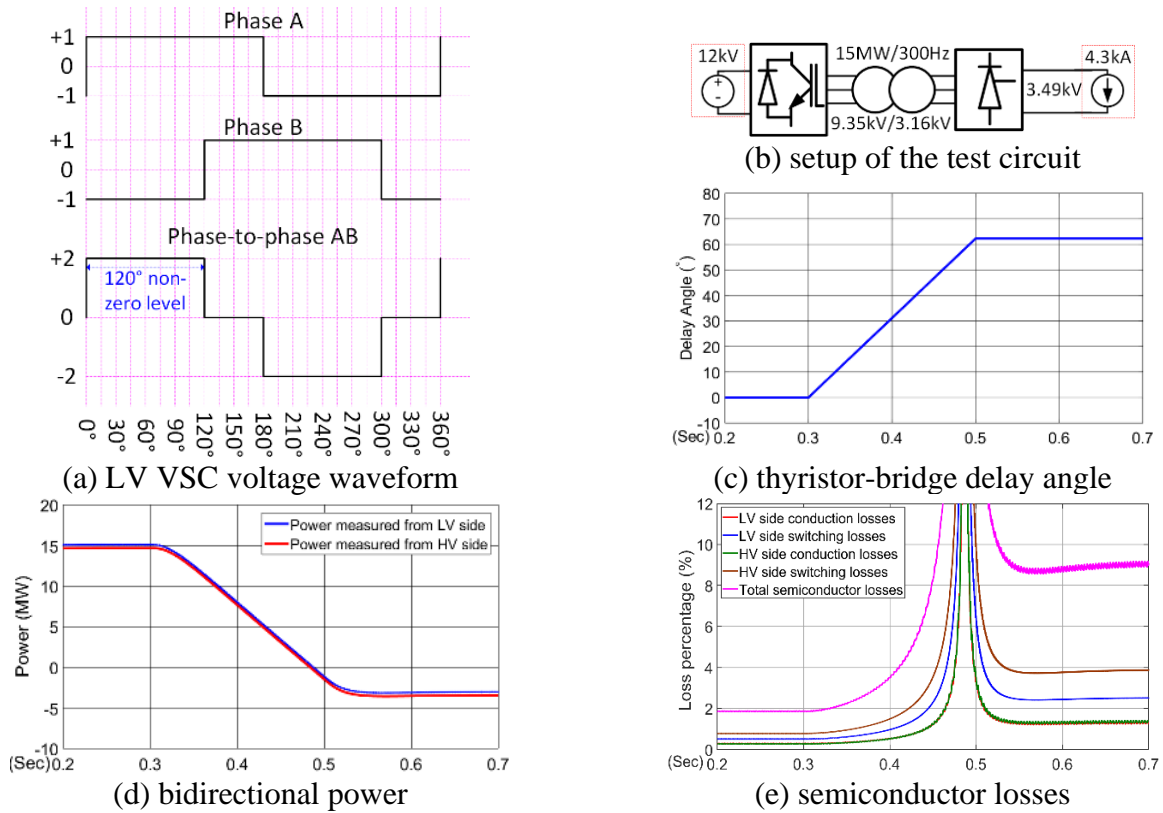Fig. 2. The dc/dc converter based on thyristor-bridge with T4771N.

(a) LV VSC voltage waveform

(b) setup of the test circuit

(c) thyristor-bridge delay angle

(d) bidirectional power

(e) semiconductor losses

Fig. 3. Simulation of the proposed dc/dc converter with thyristor CSC bridge.

The study aim is to maximize the operating frequency, while the safe commutation will be ensured by setting the extinction angle γ in (3) larger than the angle of the thyristor turn-off time T_{ex} in one fundamental

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cycle, considering the worst case inverter operating point at the maximum control angle α. Fortunately, for wind turbine applications, the reverse power demand is only a fraction of the rated power, allowing a narrow α angle range, and thus, larger safe commutation margin.

$$\gamma = 120° - (\alpha + T_\mu \cdot f_o \cdot 360°) \geq T_{ex} \cdot f_o \cdot 360° \tag{3}$$

It is seen that the turn-off time of thyristor is a critical design constraint and hence we have selected low-voltage thyristor T4771N with low T_{ex}=250μs. In the design case of Fig. 2, we have obtained an operating frequency f_o of 300Hz for an initial demonstration of the converter performance (semiconductor-level limiting factors, e.g., repetitive *di*/*dt* and switching energy for high-capacity silicon thyristors will not be considered at this stage). In this scheme, the 250μs extinction time of the chosen thyristor T4771N represents 27° in a full power cycle. Using the fundamental voltage components of the two windings, the transformer ratio is determined as 9.35kV/3.16kV (N_t=0.338), and its leakage reactance is 0.2 per unit. Therefore, the nominal output of thyristor-bridge 3.49kV/4.3kA (15MW) can be produced at around α=0° and the commutation overlap T_μ is approximately 150μs, or 16.2° at 300Hz, from (1) and (2). The power demand will range from the rated 15MW to -3MW (20%), and the corresponding delay angle α is thereby 0°~62.3° based on (1) and (2). Then, using (3), the angle protection margin γ will be 41.5° that is sufficient for the assumed device (27°). However, due to the sole use of firing delay angle control with fixed VSC voltage, the internal transformer power factor at partial load is low. Table 1 summarizes the requirement of the semiconductor devices for the CSC bridge.

Table 1. Power semiconductor effort of the thyristor-bridge.

Thyristor type	Voltage stress	Current stress	Total switch count
T4771N (2.2kV/4.3kA)	4.1kV per valve	4.3kA	24 (4 in series per valve, 6 valves)

The ac voltage supplied by the LV side 2L-VSC is a square wave in phase-to-ground as in Fig. 3(a) and the solid black line in Fig. 4. With the zero-angle reference in Fig. 4, the voltage waveform satisfies the odd half-wave-symmetry, so its Fourier series with only odd harmonics can be expressed by (4) where $\omega = 2\pi f_o$.

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The current waveform in the ac link generated by the thyristor CSC is shown as the solid blue line in Fig. 4. It has a conduction angle of 120° in each half-cycle and the position is determined by the delay angle α that is referenced to the VSC voltage. The slope time (caused by commutation overlap) is T_u determined by (1). The Fourier series of such current waveform is given in (5), and the coefficients are derived as in (6) and (7) using the parameter T_a of (8).
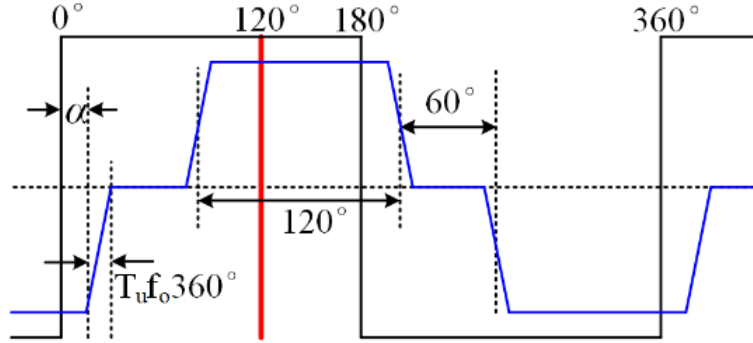

Fig. 4. The thyristor-based CSC ac current with delay angle α against the 2L-VSC voltage.

$$v_{abc.vs} = \sum_{k=1.3.5\ldots} \frac{2N_t V_{dc.vs}}{k\pi} \sin(k\omega t) \tag{4}$$

$$i_{abc.cs} = \sum_{k=1,5,7\ldots} [a_k \cos(k\omega t) + b_k \sin(k\omega t)] \tag{5}$$

$$a_k = \frac{2I_{dc}}{\pi\omega T_u k^2} \{\cos[k\omega(T_\alpha + T_u)] - \cos(k\omega T_\alpha) + \cos[k\omega(T_\alpha + T_u) + \frac{k\pi}{3}] - \cos(k\omega T_\alpha + \frac{k\pi}{3})\} \tag{6}$$

$$b_k = \frac{2I_{dc}}{\pi\omega T_u k^2} \{\sin[k\omega(T_\alpha + T_u)] - \sin(k\omega T_\alpha) + \sin[k\omega(T_\alpha + T_u) + \frac{k\pi}{3}] - \sin(k\omega T_\alpha + \frac{k\pi}{3})\} \tag{7}$$

$$T_\alpha = \frac{\alpha}{360° \times f_o} \tag{8}$$

With (4) and (5), the active and reactive power contributed by the fundamental and harmonic components can be obtained, which is critical for the design of the MFT. In this paper, only fundamental component is used to analyze the power factor, active power, and reactive power of internal ac-link, as in (9)-(11).

$$i_{1abc.cs} = a_1 \cos(\omega t) + b_1 \sin(\omega t) = I_1 \sin(\omega t + \varphi) \tag{9}$$

$$\begin{cases} I_1 = \sqrt{a_1^2 + b_1^2} \\ \cos\varphi = \frac{b_1}{I_1} \\ \sin\varphi = \frac{a_1}{I_1} \end{cases} \tag{10}$$

$$\begin{cases} P_1 = \frac{3}{2} \times \frac{2 N_t V_{dc.vs}}{\pi} \times I_1 \cos\varphi \\ Q_1 = \frac{3}{2} \times \frac{2 N_t V_{dc.vs}}{\pi} \times I_1 \sin\varphi \end{cases}$$ (11)

The calculations from (4) and (5) for harmonics components show that the power contribution form the lowest order 5th harmonic is only 3.64% of the fundamental power, while the 7th harmonic contributes only 1.73%. Therefore, because of small impact and for brevity, the harmonic power flow is not further analyzed.
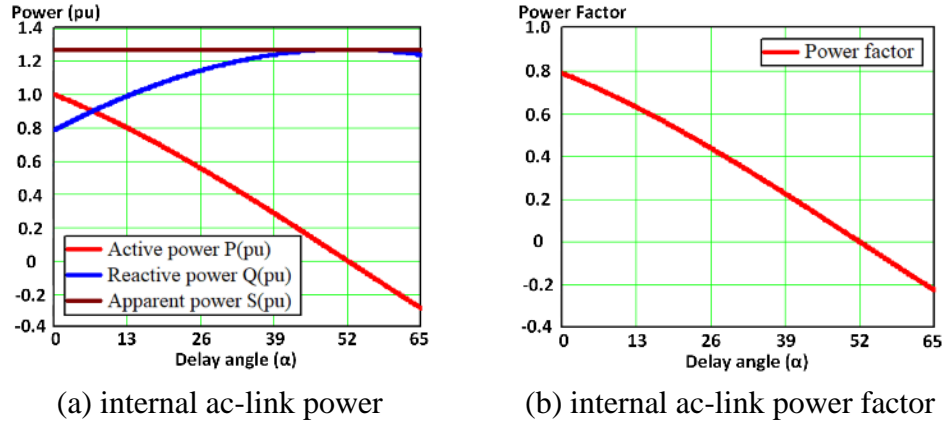

(a) internal ac-link power   (b) internal ac-link power factor

Fig. 5. The analytical results for the internal ac-link power and power factor of the 2L-VSC and thyristor CSC F2F dc/dc converter.

The converter model of Fig. 2 is implemented and simulated in PSCAD by synchronizing the thyristor-bridge delay angle α directly against the VSC square wave voltage control signal as in Fig. 3(a) or Fig. 4 (no phase locked loop). In Fig. 3(b), a 12kV dc voltage source and a 4.3kA dc current source are connected to emulate the generator ac/dc converter and the array current. The control angle α in Fig. 3(c) varies from 0° to 62.3° to ramp the power from 15MW to -3MW as observed in Fig. 3(d). Using the manufacturer datasheets for the selected IGBT and thyristor, Fig. 3(e) shows the online calculated total semiconductor loss and its breakdown at worst-case 4.3kA transmission current [23]. The loss estimation method and the parameter extraction are explained in the appendix. It is seen that losses at 0-7MW are unfavorable, caused by poor power factor. To illustrate key importance of power factor, we substitute the design parameters in Fig. 2 and Table 1 into the analytical equations (4)-(11), and the power distribution with different delay angle α can be depicted in Fig. 5. At the rated power of 15MW (1.0pu), more than 0.75pu reactive power circulation is needed with the apparent power at about 1.25pu. The maximum power factor is 0.8, and it will decrease to 0 and then reverse its sign once back-feeding is initiated since power control is based solely on delay angle.

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The corresponding simulation results on a detailed PSCAD model (incorporating switch extinction angle) are summarized in Fig. 6 and Fig. 7. During power reversal, the LV side VSC needs to change its dc current direction under constant voltage as seen from Fig. 6(a); while in Fig. 6(b), the HV side CSC reverses the polarity of its dc voltage with constant dc current. Furthermore, the zoomed-in version of ac-link voltage and current for phase A are shown in Fig. 7, confirming both 15MW and -3MW operation.
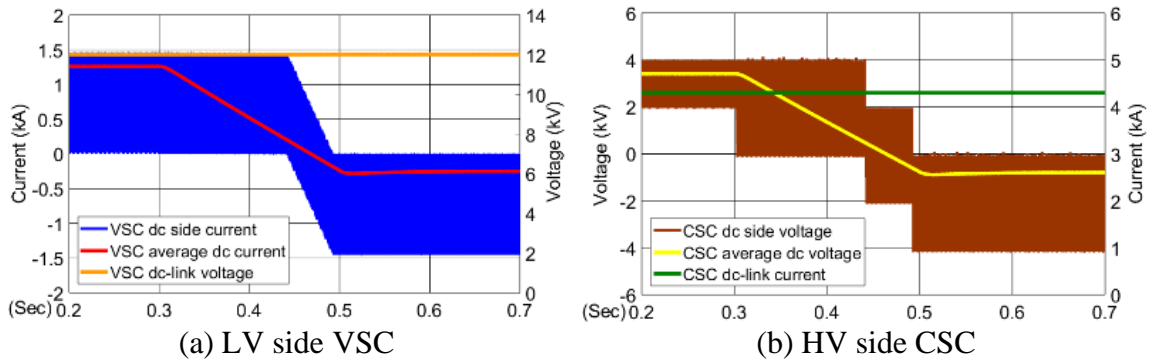

(a) LV side VSC   (b) HV side CSC

Fig. 6. The dc voltage and current (with average version).

(a) at rated 15MW   (b) at reversed 3MW
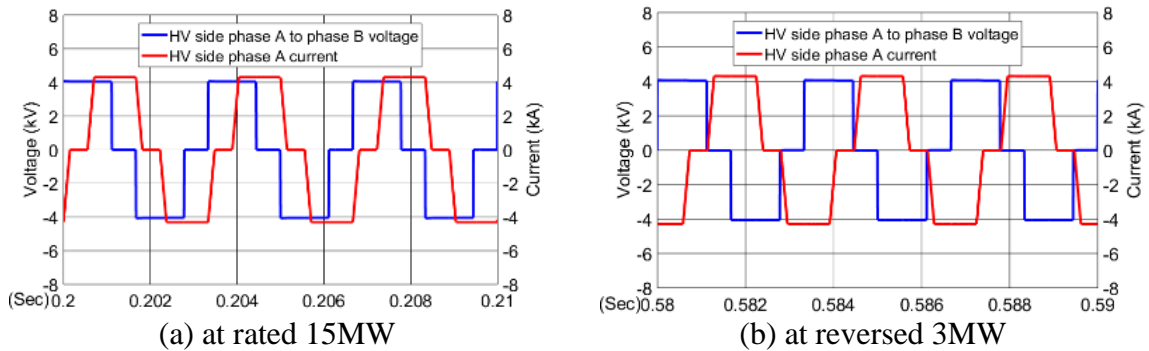
Fig. 7. Zoomed-in ac-link voltage and current (phase A, HV side).

B. DC/DC with thyristor-based CSC and 3-Level (3L) VSC

It would be beneficial to employ additional VSC ac voltage control that can offer lower switching losses, reduced reactive power circulation in the internal ac-link, extended thyristor safe commutation margin, optimized transformer design, and higher operating frequency.

The simplest option would be 2L-VSC voltage control using additional switching, but this would produce zero-level phase-to-phase voltage that violates the safe commutation of the thyristor-bridge, while the possible use of additional filters following a 2L-VSC is not preferred due to inadequate separation between the allowable switching frequency and the fundamental power frequency. Thus, the staircase ac voltage is

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recommended here, and Fig. 8 shows the proposed dc/dc converter based on the thyristor-bridge CSC and T-type 3L-VSC. The neutral-point-clamped (NPC) leg of the T-type bridge is a bidirectional switch and can be implemented by 3 series back-to-back 3.3kV/1.8kA IGBT 5SNA 1800E330400 from ABB (shown in pink in Fig. 8); while the main legs remain the same as in Fig. 2 with minimal modification of the bridge 2.

It is important to discuss the synchronization scheme of the thyristor-bridge CSC against such multilevel topology and the optimal power control method. The proposal is to exploit the non-zero intermediate level in the five-level (5L) phase-to-phase voltage to adjust its magnitude, as shown in Fig. 9 for 3 values of angle τ. A particular assumption is that the generator interfacing converter (bridge 1 in Fig. 1) will also employ the NPC topology such that the effort for balancing the neutral point voltage will be assigned to the generator side converter operating with low power frequency. In this way, the NPC bridge inside the dc/dc converter (bridge 2 in Fig. 1) can have minimized switching frequency and losses.
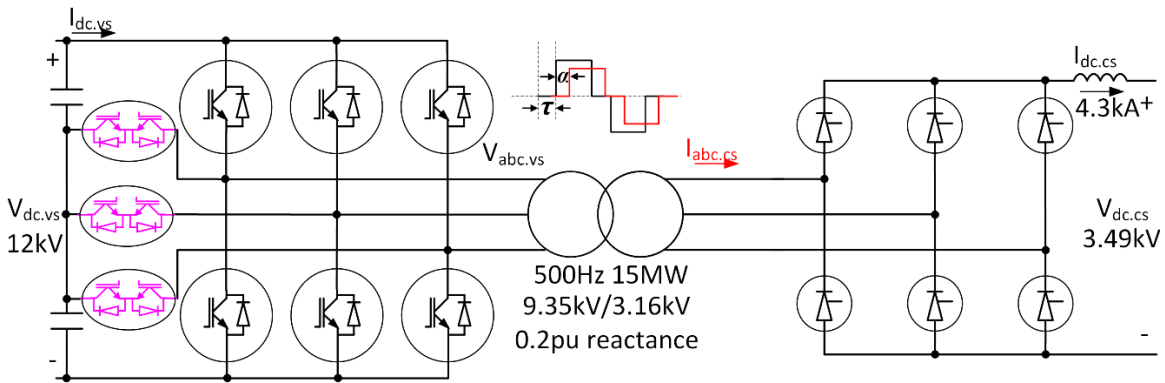

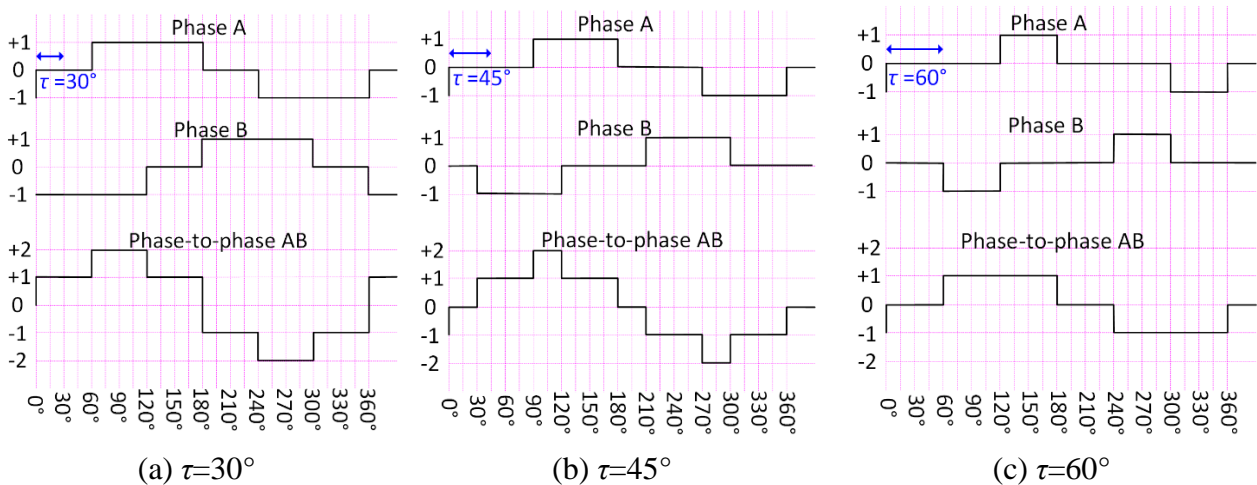Fig. 8. The dc/dc converter based on thyristor-bridge and T-type 3L-VSC.

(a) τ=30°   (b) τ=45°   (c) τ=60°

Fig. 9. The T type VSC voltage waveforms under non-zero control angle τ.

As illustrated in Fig. 10, the two control degrees of freedom, α and τ, can be combined to achieve optimized operating trajectory with power load variation. As a recommendation, the NPC-VSC will operate with $\tau=30°$ at full power generation, and the thyristor-bridge delay angle α is set at zero. Then, to reduce the power, the zero-level angle τ of NPC-VSC can be increased to lower the voltage magnitude. During this process, the natural commutation point position of thyristor-bridge (when positive rising edge of phase-to-phase voltage occurs) will move relative to the 0° reference defined in Fig. 10. This is described by α_0 in (12), and any CSC delay angle control will be superposed to α_0.

$$\alpha_0 = 2(\tau - 30°), with\ 30° \leq \tau \leq 60° \tag{12}$$

As τ angle is increasing, the phase-to-phase voltage waveform will be kept 5L until the boundary case of Fig. 9(c) with $\tau=60°$, when the ac voltage magnitude is halved and phase-to-phase voltage waveform degenerates into 3L (same as for a 2L-VSC). Further increase of τ should be avoided as it would lead to unwanted zero voltage level at the center position of the phase-to-phase voltage waveform, which can violate the safe commutation criteria of the thyristors. Thus, to further reduce and reverse the power, CSC side delay angle control will be initiated. According to (12), the non-zero phase-to-phase voltage pulse width A_{n0} (maximum thyristor-bridge delay angle) is given in (13), which is higher than that for the 2L-VSC until $\tau=60°$. In addition, the voltage reduction by τ angle control allows the power frequency to reduce proportionally (constant transformer flux), so that the thyristor CSC enjoys an extended safe commutation margin. The reduced power frequency also benefits in lower losses and lower reactive power circulation in part-load conditions.

$$A_{n0} = 180° - 2(\tau - 30°), with\ 30° \leq \tau \leq 60° \tag{13}$$

The reference voltage that the thyristor-bridge synchronizes against is shown as the black solid line in Fig. 10, based on the modulation of the NPC-VSC. Its Fourier series is derived as in (14) with the coefficients shown in (15) and (16). T_τ and the variation of the power frequency ω (or f_o) are defined in (17), where the frequency linearly decreases from its rated level with a rate equal to the ratio of the transformer excitation voltage magnitude (volt-second area) as controlled by the modulation angle τ in Fig. 10. The blue solid line

is the CSC ac current, and its Fourier series waveform inherits that from (5)-(7) with T_u now being twice of that in (1) due to the halved commutation voltage level along the recommended operating trajectory. If the 3L-VSC fundamental voltage is expressed in (18), combined with the current expressions in (9) and (10), the internal ac-link power and power factor for the proposed 3L-VSC and thyristor CSC F2F dc/dc converter can be obtained as shown in (19) and (20).
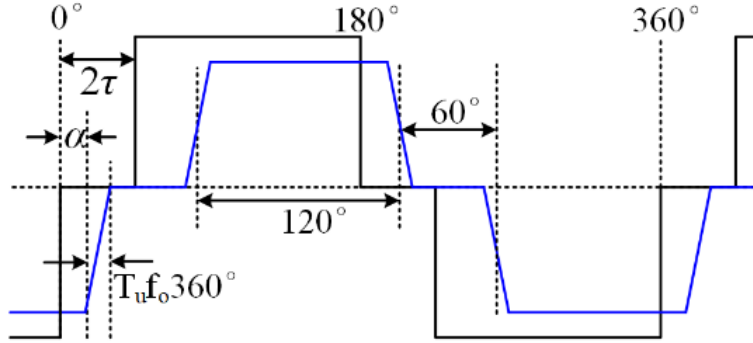

Fig. 10. The thyristor-based CSC ac current with delay angle α against the NPC-VSC voltage.

$$v_{abc.3Lvs} = \sum_{k=1,3,5...}[c_k \cos(k\omega t) + d_k \sin(k\omega t)] \tag{14}$$

$$c_k = \frac{N_t V_{dc.vs}}{2k\pi}[\sin(2k\omega T_\tau + k\pi) - \sin(2k\omega T_\tau)] \tag{15}$$

$$d_k = \frac{N_t V_{dc.vs}}{2k\pi}[\cos(2k\omega T_\tau) - \cos(2k\omega T_\tau + k\pi) + 2] \tag{16}$$

$$\begin{cases} T_\tau = \frac{\tau}{360 f_o} \\ \omega = \omega_{rated} \cdot \frac{90° - \tau}{60°} \end{cases}, with\ 30° \leq \tau \leq 60° \tag{17}$$

$$v_{1abc.vs}^{3L} = c_1 \cos(\omega t) + d_1 \sin(\omega t) = V_1^{3L} \sin(\omega t + \delta) \tag{18}$$

$$\begin{cases} V_1^{3L} = \sqrt{c_1^2 + d_1^2} \\ \cos(\delta - \varphi) = \frac{b_1}{I_1} \cdot \frac{d_1}{V_1^{3L}} + \frac{a_1}{I_1} \cdot \frac{c_1}{V_1^{3L}} \\ \sin(\delta - \varphi) = \frac{b_1}{I_1} \cdot \frac{c_1}{V_1^{3L}} - \frac{a_1}{I_1} \cdot \frac{d_1}{V_1^{3L}} \end{cases} \tag{19}$$

$$\begin{cases} P_1 = \frac{3}{2} \times V_1^{3L} \times I_1 \cos(\delta - \varphi) \\ Q_1 = \frac{3}{2} \times V_1^{3L} \times I_1 \sin(\delta - \varphi) \end{cases} \tag{20}$$

Considering the extreme case in terms of thyristor safe commutation range and switching losses using the proposed variable ac voltage and frequency operating mode, in Fig. 8, the upper limit of 500Hz for the

operating frequency range is chosen under the rated power of 15MW, while the limitations such as the

thyristor repetitive *di/dt* are not considered in this paper. Substituting the design parameters of Fig. 8 into

(19) and (20), the analytical results for internal ac-link power can be plotted in Fig. 11. It is observed that

the active power can be reduced to half-rated level by increasing the 3L-VSC control angle τ from 30° to

60°, and the associated reactive power circulation is significantly lower than that for the 2L-VSC method

shown in Fig. 5. After τ is fixed at 60°, the thyristor-bridge delay angle is used to further bring power down

to zero and then reverse its direction to -0.2pu. In this delay angle control phase, the power factor is the same

case as for Fig. 5, but the apparent power capacity (also reactive power) in low power generation region is

halved compared to that in Fig. 5.

(a) power *vs.* τ angle

(b) power *vs.* α angle

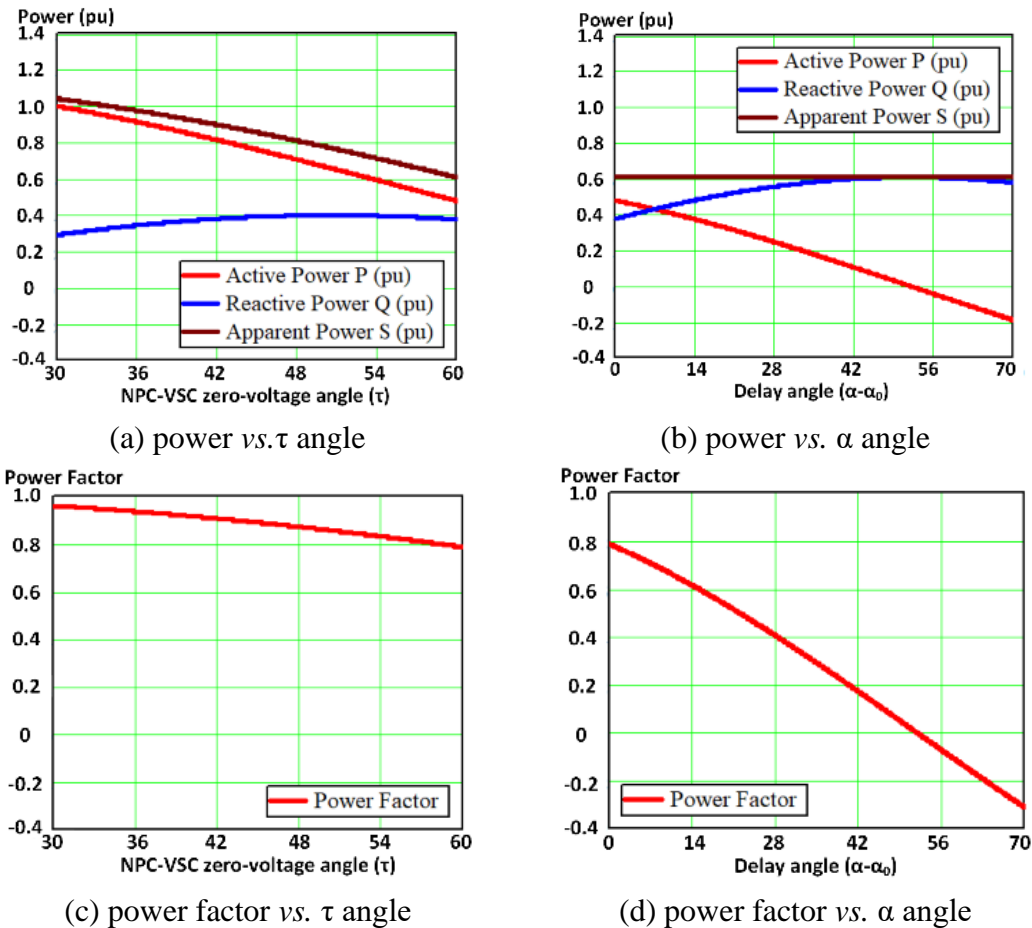(c) power factor *vs.* τ angle

(d) power factor *vs.* α angle

Fig. 11. The analytical results for the internal ac-link power and power factor of the 3L-VSC and thyristor CSC F2F dc/dc converter.

As a verification, the operational principle of the proposed converter is simulated by PSCAD as arranged

in Fig. 12. Initially, the power is established at the rated 15MW with zero delay angle for the CSC and the

VSC operates at 30° τ angle, as seen in Fig. 12(b)-(e). After 0.3s, NPC-VSC starts to reduce the voltage magnitude until the half-rated level (also the power) at 0.4s when $\tau=60°$, and the frequency is proportionally reduced to 250Hz. The ac voltage will then be fixed, and from 0.4s, the CSC delay angle control is activated to further reduce the power to zero and reverse it to -3MW at around 0.5s. Fig. 12(f) shows the online calculation of the total semiconductor loss and its breakdown (the worst-case scenario with fixed and highest dc transmission current). It is observed that the switching loss at full power is similar to (marginally lower than) that of Fig. 3(e) even 500Hz is assumed, which is due to the use of reduced commutation voltage (lower di/dt) by the 3L-VSC. Then, the switching loss becomes much lower than the Fig. 3(e) case if power (either direction) is below the half-rated level. This is explained by the reduced power frequency. The loss curves in Fig. 12(f) will be globally downshifted if a 300Hz or lower rated power frequency is used.

(a) setup of the test circuit

(b) NPC-VSC zero-level angle

(c) power frequency

(d) thyristor-bridge delay angle α-α₀
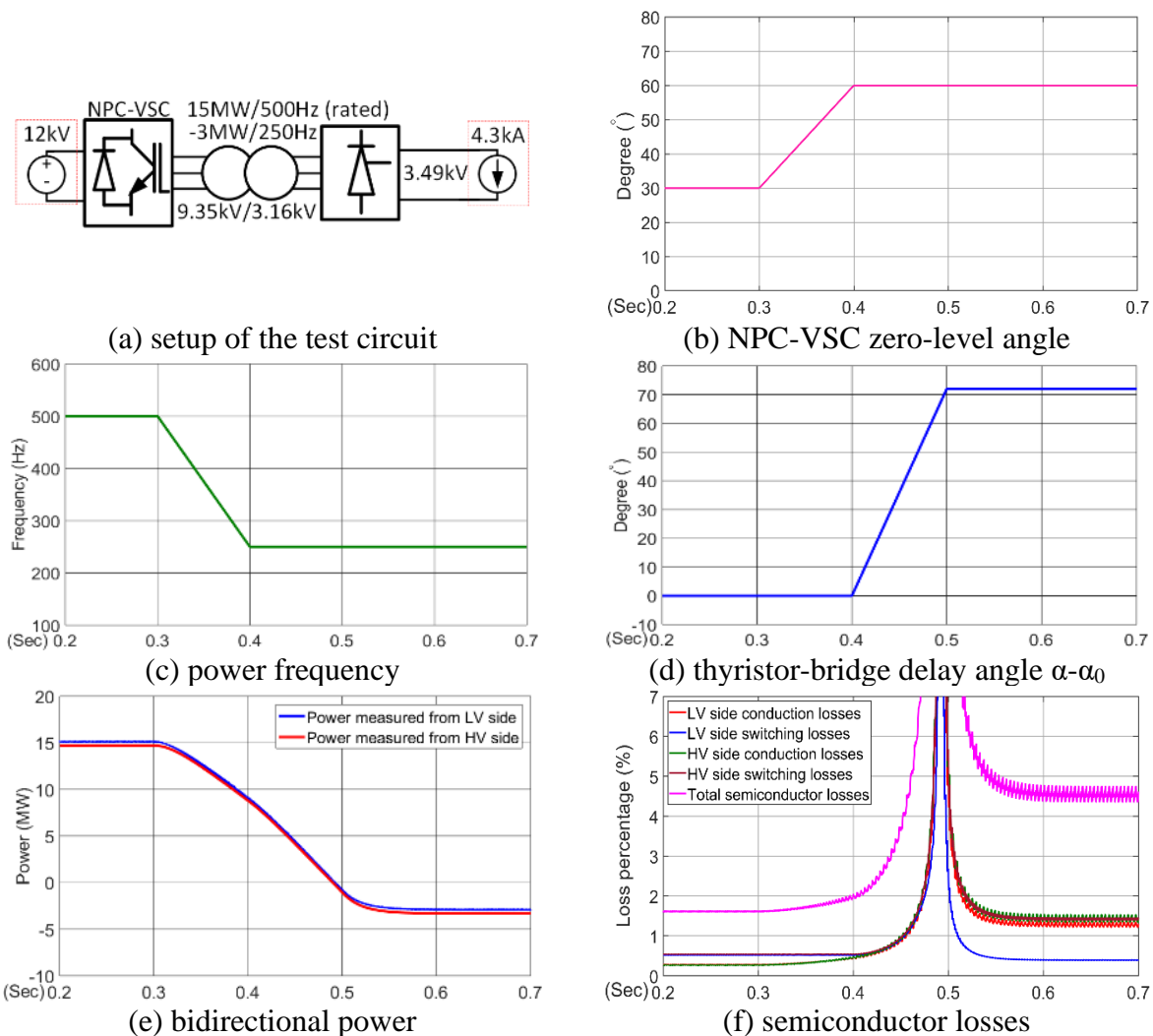
(e) bidirectional power

(f) semiconductor losses

Fig. 12. Simulation of the proposed dc/dc converter based on the thyristor bridge and NPC VSC.

Fig. 13 presents the dc voltage and current profiles at both the VSC and CSC sides during the power reduction and reversal process. It is seen that, by using 3L-VSC, the harmonics at CSC dc side are substantially lower compared to the case with 2L-VSC in Fig. 6(b). The zoomed-in ac-link voltage and current of the phase A under rated power and 500Hz is displayed in Fig. 14(a). The 5L phase-to-phase waveform in Fig. 14(b) is varied to control the voltage and power. In Fig. 14(c), the minimum required voltage for the safe commutation of the thyristor-based CSC is reached with halved operating frequency (250Hz); and the power reversal to -3MW is displayed in Fig. 14(d) by the CSC side delay angle control.
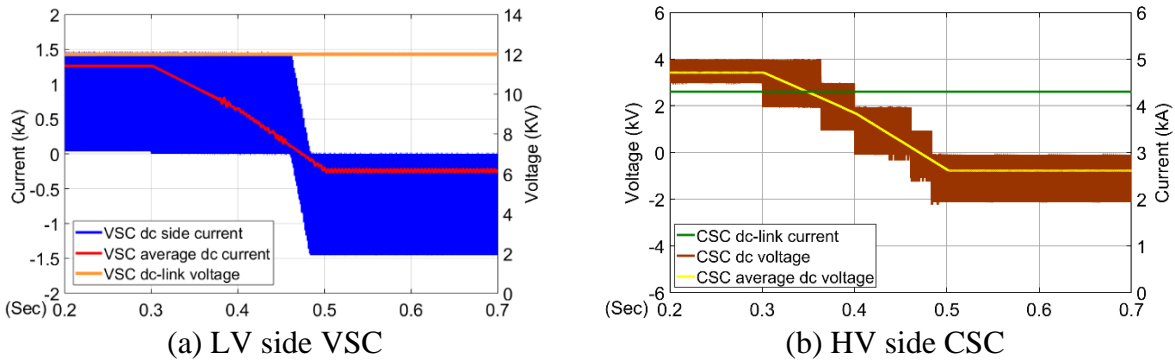

(a) LV side VSC

(b) HV side CSC

Fig. 13. The dc voltage and current (with average values).

(a) at rated 15MW with 500Hz

(b) at reduced voltage and power

(c) at half voltage and power with 250Hz

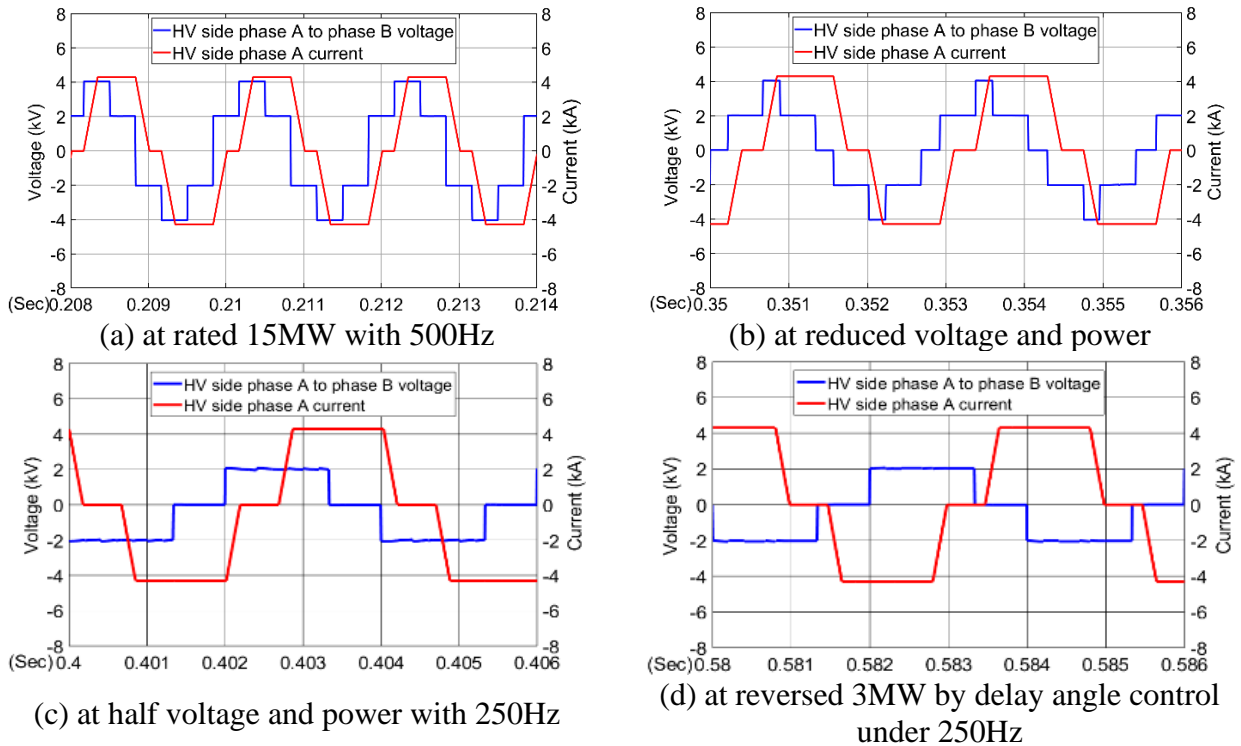(d) at reversed 3MW by delay angle control under 250Hz

Fig. 14. Zoomed-in ac-link voltage and current (phase A, HV side).

C. DC/DC with self-commutated CSC

The CSC bridge can also be built based on self-commutated symmetrical power switches, e.g., SGCT/SGTO or IGBT with RB-diode, with the latter option offering good choice of standard switches and faster switching speed. Based on the ABB 4.5kV/3kA IGBT 5SMA 3000L450300 and 4.5kV/2.6kA fast recovery diode 5SDF 28L4521, a 4-parallel-16-series 96kV/960MW wind farm is formed, i.e., $m=4$, $n=16$ for Fig. 1. The design of such dc/dc converter using a 2L-VSC is shown in Fig. 15, and its ac-link waveforms are shown in Fig. 16, where the two sides can be viewed as independent voltage and current sources with arbitrary phase-shift angle θ.
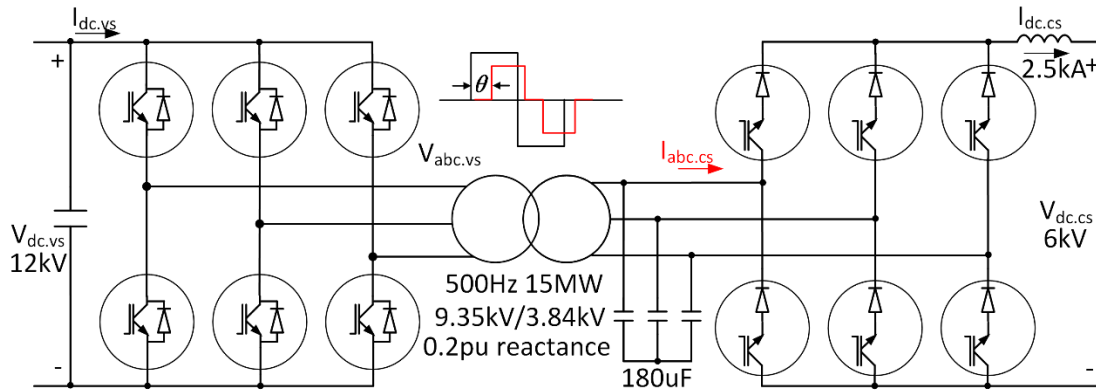

Fig. 15. The dc/dc converter based on IGBT plus RB-diode CSC-bridge with 5SMA 3000L450300 and 5SDF 28L4521.

The Fourier series for the voltage waveform in Fig. 16 is the same as (4), while the current waveform (assuming zero current commutation time) is expanded as (21) with the coefficients in (22) and (23).
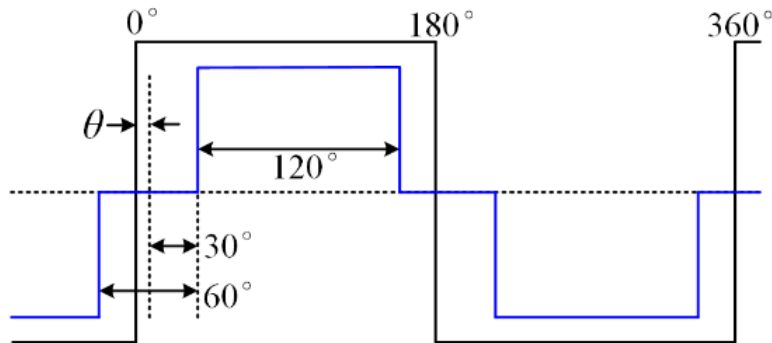

Fig. 16. The self-commutated CSC ac current with phase-shift angle θ against the 2L-VSC voltage.

$$i_{abc.cs.s} = \sum_{k=1,3,5\ldots}[e_k \cos(k\omega t) + f_k \sin(k\omega t)] \tag{21}$$

19

$$e_k = \frac{2I_{dc.cs}}{k\pi}\left[\sin\left(k\theta + \frac{5k\pi}{6}\right) - \sin\left(k\theta + \frac{k\pi}{6}\right)\right] \tag{22}$$

$$f_k = \frac{2I_{dc.cs}}{k\pi}\left[\cos\left(k\theta + \frac{k\pi}{6}\right) - \cos\left(k\theta + \frac{5k\pi}{6}\right)\right] \tag{23}$$

Due to the presence of the shunt capacitors in the ac-link, the per-phase equivalent circuit can be described by Fig. 17, with L_t and Cs being the transformer leakage inductance and the shunt capacitance in star-connection. In addition, the terms $v_{vs.k}$, $v_{cs.k}$, and $i_{cs.k}$ are used to represent the kth order component of the VSC voltage, capacitor voltage, and CSC current, respectively. Then, the shunt capacitor C_s voltage $v_{cs.k}$ can be solved as (24), based on the Fourier format expressions of the 2L-VSC voltage and self-commutated CSC current in (4) and (21). In the same way, the inductor current can be obtained for the power analysis of the VSC. The practical design process will be iterative to consider multiple requirements including: the passive component size, reactive power capacity, and harmonic ingredients. In Fig. 15, the transformer is finally selected to be 9.35kV/3.84kV with 0.2pu leakage reactance; and the capacitor in start-connection is 180μF. Substituting these design parameters into (21)-(24), the analytical waveform of capacitor voltage can be estimated using the fundamental, 5th, and 7th order components. The phase-to-phase version of such voltage along with the CSC side current is shown in Fig. 18 with the phase-shift angle being 0° and 100° for 15MW and -3MW, respectively.
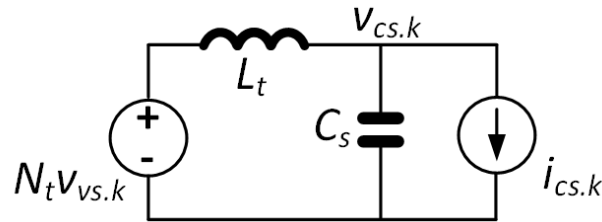

Fig. 17. The internal ac-link equivalent circuit using self-commutated CSC.

$$V_{cs.k} = \frac{N_t V_{vs.k} - jk\omega L_t \cdot i_{cs.k}}{1-(k\omega)^2 L_t C_s} = \frac{\frac{2N_t V_{dc.vs}}{k\pi}\sin(k\omega t) - k\omega L_t \cdot [f_k \cos(k\omega t) - e_k \sin(k\omega t)]}{1-(k\omega)^2 L_t C_s} \tag{24}$$

From equation (24) and Fig. 18, the shunt capacitor voltage can be calculated as no more than 8kV (phase-to-phase peak value), so the semiconductors requirement is summarized in Table 2. Compared to the thyristor design in Table 1, it is seen that the use of IGBT with series diode will require larger semiconductor area (both IGBTs and diodes) and incur higher cost (including driver costs).

20

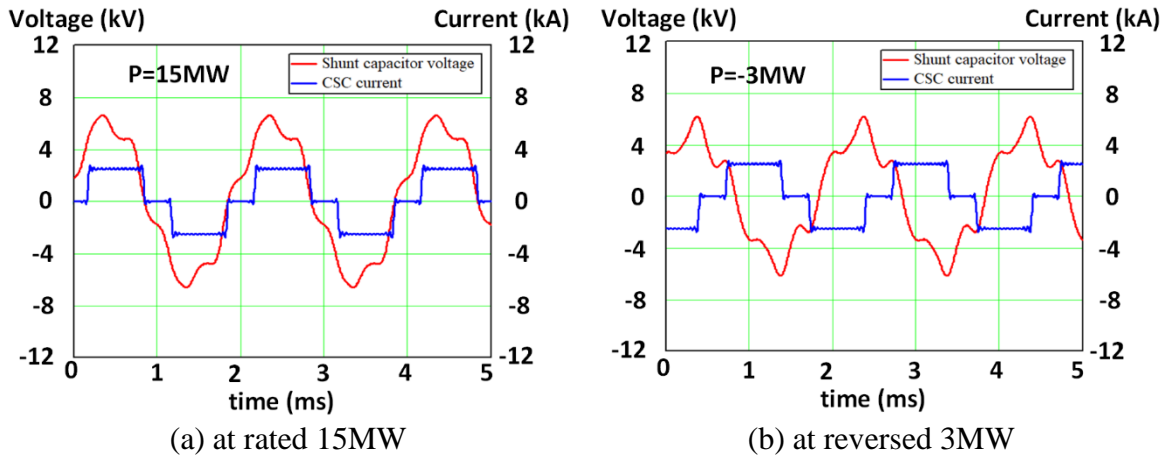(a) at rated 15MW   (b) at reversed 3MW

Fig. 18. The analytical results of the ac-link voltage and current for the self-commutated CSC.

Table 2. Power semiconductor effort of the IGBT plus RB diode CSC-bridge.

IGBT/Diode type	Voltage stress	Current stress	Total switch count
5SMA3000L450300 (4.5kV/3kA)	<8kV per valve	2.5kA	18 (3 in series per valve, 6 valves)
5SDF 28L4521 (4.5kV/2.6kA)	<8kV per valve	2.5kA	18 (3 in series per valve, 6 valves)

The PSCAD model and simulation results are presented in Fig. 19, assuming 500Hz frequency. The power factor angle of the VSC and CSC is varied to control the power from the rated 15MW to reversed 3MW as observed from Fig. 19(b)-(c). With the datasheet parameters, the power losses are calculated in Fig. 19(d), and the high partial power losses is observed under the worst-case scenario (highest dc current). Considering that the allowable frequency is not adequately higher than the fundamental power frequency, the use of VSC voltage magnitude control (2L-VSC with additional switching angle or 3L-VSC) in an effort to optimize the ac-link power factor may complicate the selection of shunt capacitance as extra control variable emerge in (24). Also, with the shunt capacitor, reduced power frequency at low generation is not recommended. These factors make the optimization of this converter rely on the design trade-off such as between the rated dc current level and operating flexibility (voltage share per generator in the series string), rated power frequency and converter size. Moreover, the system-wide dc current management will benefit the efficiency in full range. The adoption of SGCT/SGTO in the CSC bridge may also reduce the losses.
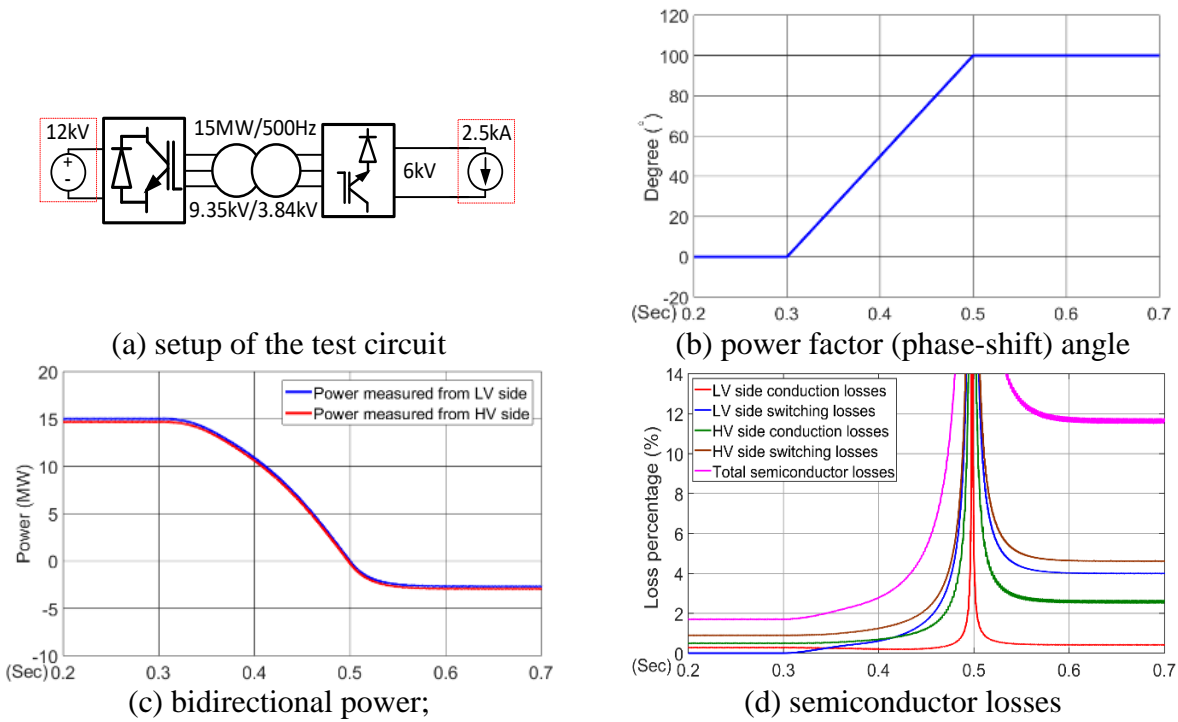
(a) setup of the test circuit

(b) power factor (phase-shift) angle

(c) bidirectional power;

(d) semiconductor losses

Fig. 19. Simulation of the proposed dc/dc converter with self-commutated CSC.

(a) LV side VSC

(b) HV side CSC

Fig. 20. The dc voltage and current (with average version).

(a) at rated 15MW
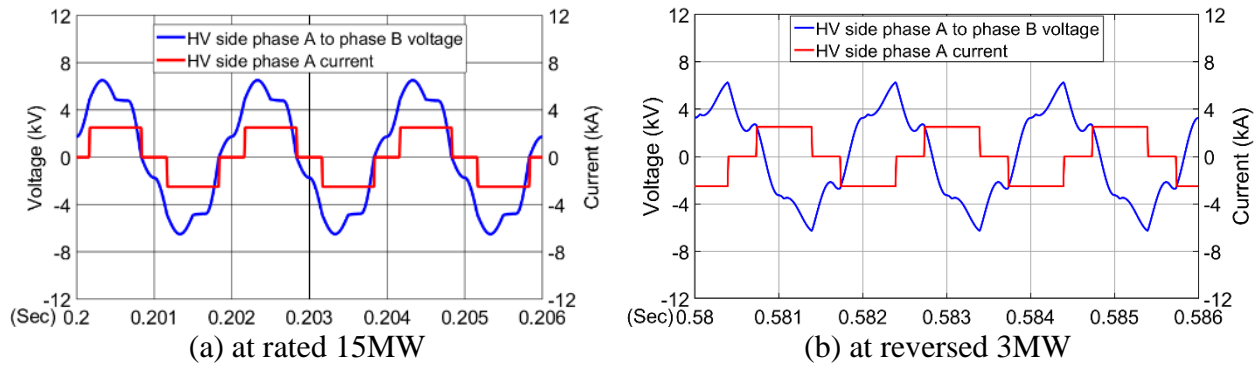
(b) at reversed 3MW
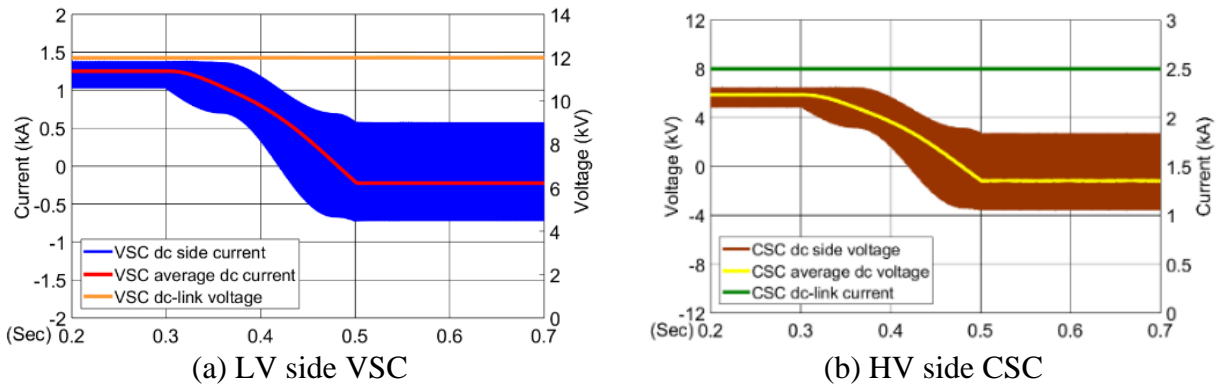
Fig. 21. Zoomed-in ac-link voltage and current (phase A, HV side).

The dc voltage and current of both sides during bidirectional power flow can be observed in Fig. 20. In addition, the internal ac-link voltage and current waveforms for phase A are zoomed in as in Fig. 21, which agrees well with the calculation results of shunt capacitor voltage in Fig. 18 and (24).

D. DC/DC converter insulation

Fig. 22 shows the proposed insulation method for the dc/dc converter in a series array. The generator and LV side converters are rated for standard voltage and can be grounded as in any other wind generator. The transformer provides galvanic isolation, and on the HV side, the transformer windings and CSC bridge are rated for medium voltage but require 100kV insulation to the ground. An insulating platform is used to support all HV components as it is common practice with many series-connected devices in power system such as the thyristor-controlled-series-capacitor (TCSC), from the family of the flexible ac transmission system (FACTS) devices. The dc cable and bushings should be rated for 100kV insulation.
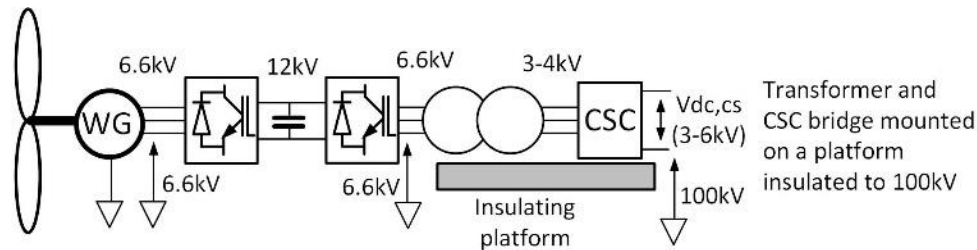

Fig. 22. Insulation of the series-connected dc/dc converter.

E. Reverse power flow for the whole wind farm

During the wind calm periods, or generator downtime, the proposed designs enable back-feeding from the onshore grid to supply all the ancillaries. Otherwise, although the onboard batteries can support for short-time essential functions such as measurement, communication, control, and heating, for any longer time, the alternative would be using offshore diesel generators that will incur high cost and negative environmental impact [24]. The power reversal with bidirectional dc/dc stage can be discussed in three scenarios:

- *Power reversal on a single generator*: the power flow on one or several generators can be reversed while others are still generating. This option can be employed for fast short-term power reversal on a limited number of wind generators. To completely disconnect the generator converter from the series array, a

mechanical bypass switch is required. In such situation, the string voltage will reduce, so the transmission voltage should be adjusted by coordinated control to ensure the power flow. If the power evacuation is low or the dc/dc converters are pre-designed with enough voltage overrating margins, the onshore converter will be allowed to maintain the transmission voltage.

- *Power reversal on the whole wind farm using dc voltage polarity reversal*: if the whole wind farm needs power reversal, the dc transmission voltage polarity should be reversed to maintain unidirectional current in the CSCs. This can be readily achieved with the onshore FB-MMC, which is required in any case with a series-connected wind farm. The main difficulty of this method is with the dc cables as the least-costly cross-linked polyethylene (XLPE) cable requires a long charge recovery time (over 10 minutes) before voltage reversal is allowed. This means the onboard batteries must have sufficient capacity before back-feeding can be initiated. Alternatively, the mass impregnated (MI) dc cable is often used with commercial HVDC transmission up to 600kV and can reverse dc voltage instantaneously.

- *Power reversal on the whole wind farm using auxiliary mechanical switches*: to reverse the power flow direction of the whole wind farm, while keeping the same dc cable voltage, auxiliary mechanical switches can be installed at the terminals of each array. The power flow reversal process will need to firstly stop the current in each array, then alter the voltage polarity by using the mechanical switches, and finally increase the current to the desired level.

IV. COMPARISON WITH PARALLEL CONNECTED WIND FARM

A. *Parallel connected platform-less wind farm*

For a platform-less pure parallel-connected wind farm, the generator dc/dc converter should be of single step-up stage with compact design to fit into the tower or nacelle.

Since bidirectional power flow is assumed in this study, the secondary side of the parallel dc/dc converter must be an active bridge that sustains the full transmission voltage. The MMC type topologies may not be preferred due to the large dc capacitors and semiconductor count for such space-confined application. Either

2L or 3L VSC could be the possible solution using power semiconductor in series, and the 2L-VSC is adopted in Fig. 23. Using standard design approach for dual-active-bridge (DAB) [25], the LV side VSC will remain the same as the series dc/dc converters, and the HV bridge semiconductor effort is shown in Table 3. It is seen that, due to the very low level of current, the 250A HV bridge IGBT modules (low-current rated commercial 6.5kV switches) have to be underutilized. It is seen that 168 IGBT switches would be needed, together with their drivers (which significantly further contribute to costs), and the cost would be much higher compared with 24 thyristors required for the dc-dc design in Table 1. It is known that IGBT module cost significantly depend on the voltage rating, and does not proportionally reduce with current rating, because of packaging and driver costs.
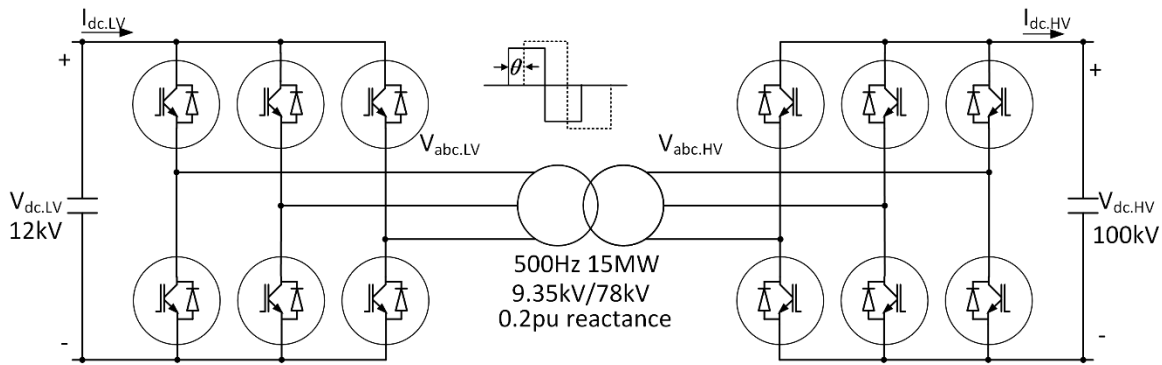

Fig. 23. The dc/dc converter based on dual-active-VSC-bridge for the parallel-connected platform-less wind farm.

Table 3. Power semiconductor effort of the HV side 2L-VSC bridge.

IGBT type	Voltage stress	Current stress	Total switch count
FZ250R65KE3 (6.5kV/250A)	100kV per valve	157A	168 (28 in series per valve, 6 valves)

The PSCAD simulation results of such high step ratio VSC DAB with classical phase-shift control is presented in Fig. 24. Both sides of VSC bridges will alter their dc current directions for bidirectional power flow. To minimize the current, the HV bridge lags the LV side by 10.8° initially under the rated 15MW power, and finally it leads the LV side by 2.2° at 3MW back-feeding, as seen in Fig. 24(b)-(c). The semiconductor losses are plotted in Fig. 24(d), where the partial load losses are similar to that for the rated

condition due to the constant high operating voltage. A significant disadvantage of this configuration is the high number of power switches with dedicated gate drivers (the gate drivers for high capacity IGBTs can cost in the same order as the main switches), which will be further deteriorated if the HV side VSC bridge (full transmission voltage rated) adopts the 3L or MMC topologies.

(a) setup of the test circuit

(b) angle between VSC voltages

(c) bidirectional power
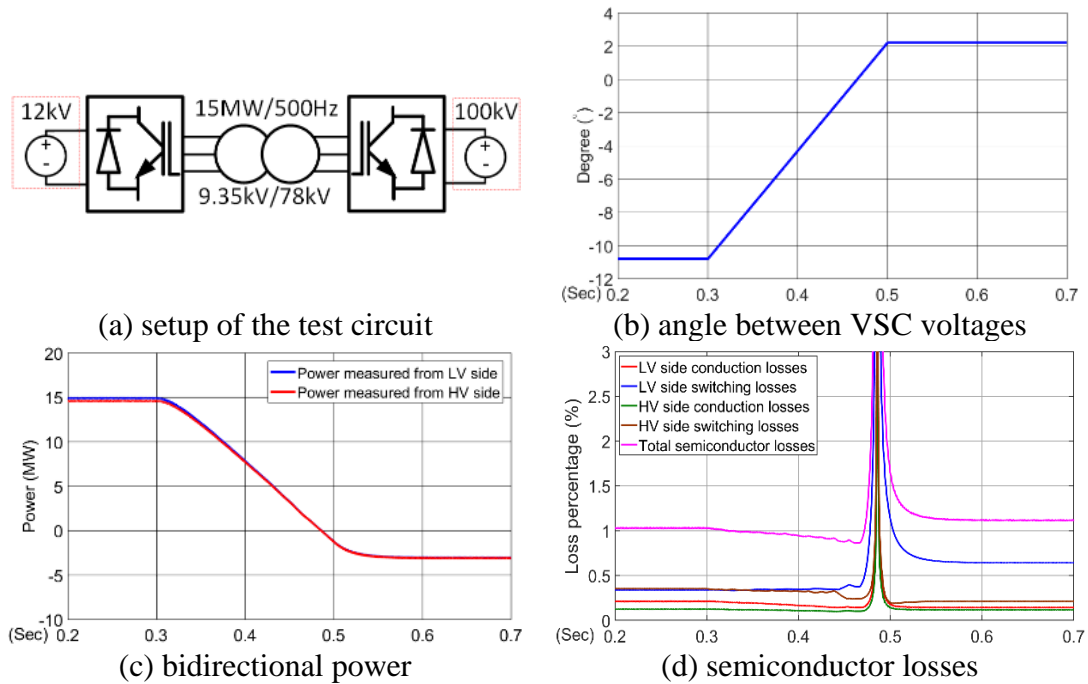
(d) semiconductor losses

Fig. 24. Simulation of the dc/dc converter with classical VSC DAB for parallel connection.

The above study clearly points to the cost advantage of using a series-connected wind farm with the assumed topology. The losses of the optimized dc/dc converter for series-connection are not significantly higher than those for the pure parallel dc/dc scheme, especially at the rated power level. By assuming superconducting cables, transmission losses will not be the decisive factor that outweighs the gains of series wind farm. The insulation effort of the series-connected dc/dc converter is also considered as standard. However, unique top-level control is required to cope with the uneven generator operating conditions in a series wind farm.

V. CONTROL OF SERIES CONNECTED WIND FARM

While detailed controller designs are out of the scope of this paper, some generic principles and strategies for the multi-array series-connected wind farm will be discussed.

If all generators in a series wind farm have identical power, it can share the same strategy as for the parallel wind farm with current control under the fixed highest dc voltage. This would significantly further reduce calculated part-load losses for the series design by lowering the string current globally.

The main operational challenge of a series wind farm is the uneven power among generators such as out of service and wind energy variation. To accommodate such challenge, there are 3 main options summarized as follows:

- *Control approach*: the current in an array will follow the demand of the highest production generator. In this way, each generator dc/dc converter can enjoy the full range of power and voltage variation. However, this means a fixed high dc current for all generators even under partial load; hence, the efficiency will drop quickly along with power reduction, and the calculations in this study assume such worst-case scenario.

- *Design approach*: the CSC bridge can be designed with voltage overrating margins that allows more space to increase the voltage share of the converter (current can be reduced if necessary), so that the transmission voltage can be maintained [26]. Obviously, this will cause increased component costs and losses at rated power.

- *Operational restriction*: if the operating flexibilities and design margins for the voltage and current are run out, the wind energy can be curtailed in order to ensure the continuous operation of the system [8], [27].

In a practical system, it is highly likely that all the 3 options will be combined to achieve full range optimal performance.

VI. Conclusion

This paper demonstrated the test case of the parallel-series-connected 1GW/100kV offshore wind farm, using single step-up dc/dc stage by series-connection and superconducting cable transmission.

As illustrated by detailed PSCAD models, it is possible to design bidirectional F2F mixed VSC and CSC dc/dc converters in several topologies. First, a thyristor-based CSC bridge can be synchronized against the fixed square wave voltage from a 2L-VSC bridge. Then, a more promising solution is proposed, based on 3L-VSC and thyristor bridge operating with a variable ac voltage and power frequency to allow improved partial load efficiency. It will also enable lower harmonics (less passive filtering) and potentially compact design (possible higher power frequency). These features are particularly important with the offshore wind generator applications. The detailed simulation on PSCAD also confirmed the performance and illustrated bidirectional power regulation based on variations in ac voltage, power frequency, and thyristor bridge delay angle. It is worth reiterating that the repetitive di/dt limit on the power frequency is not given in the commercial thyristor datasheet due to its predominant usage for the line frequency. While the medium frequency range between 200Hz~500Hz is considered in this paper, the use of 500Hz for the proposed 3L-VSC and thyristor bridge dc/dc converter is an extreme case to highlight the extent where operation flexibility and performance enhancement are possible. A separate device-level study (such as semiconductor limitations and transformer design criteria) is needed to identify practically the most appropriate power frequency selection for such converter. Alternatively, the CSC with IGBT and series RB-diode allows higher frequency operation up to 500Hz but incurs higher semiconductor costs and losses.

The comparison with parallel-connected 1GW wind farm points to significant advantages of the series wind farm in terms of the total semiconductor count and costs. In series or series-parallel wind farms, each 15MW dc-dc converter assumes only a fraction of the transmission voltage (a few kV up to 10kV), so the switch count per converter will be significantly lower than that for a pure parallel wind farm, although the current rating increases. The insulation design is not seen as a prominent difficulty compared to the parallel dc wind farm (all converters are located inside the tower on simple insulation platforms), especially if lower transmission voltage is allowed by superconducting cable technology. Challenges on the power balancing control of series-parallel dc wind farm can be addressed by coordinating the converter design and control strategy, which will be topic of further in-depth and quantitative studies.

The block diagrams for online calculating the switching and conduction losses of IGBT, diode, and thyristor within PSCAD simulation are shown in Fig. A-1, Fig. A-2, and Fig. A-3.
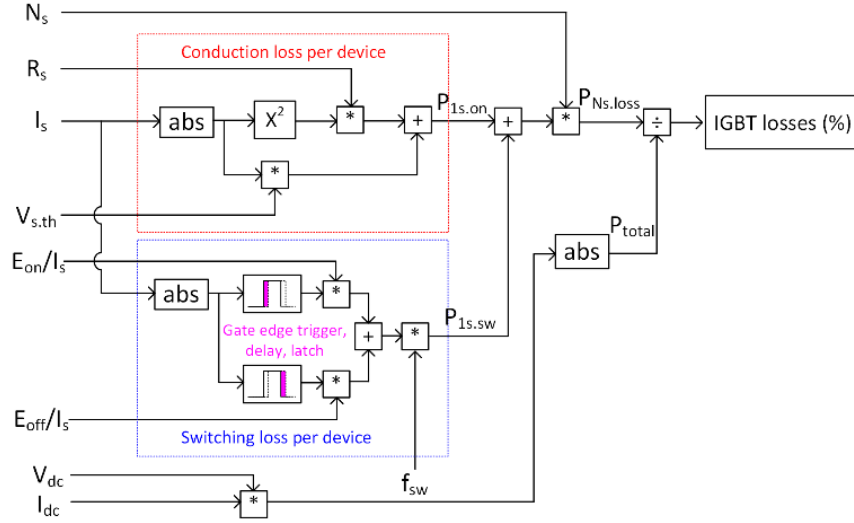

Fig. A-1. Online calculation of IGBT conduction, turn-on, and turn-off losses.

The required quantities in Fig. A-1 are as follows. N_s is the total IGBT number of the same type in the converter, Rs is the slope resistance of the IGBT. $V_{s.th}$ is the IGBT on-state voltage drop. I_s means the instantaneous current flowing in the IGBT channel. the switching energies of IGBT E_{on} and E_{off} are both functions of I_s under the given voltage, temperature, and gating condition. f_{sw} is the device switching frequency. We also use the converter V_{dc} and I_{dc} to obtain the total input power in order to get the percentage of the losses out of the total power flow. The switching instant currents for estimating E_{on} and E_{off} of the IGBT will be captured based on the relevant gate signals with manually adjusted delay blocks to ensure the accuracy. Fig. A-1 is applied to 5SNA 2000K452300 for the LV side 2L and 3L VSCs, 5SNA 1800E330400 for the 3L-VSC NPC leg, the self-commutated CSC bridge IGBT 5SMA 3000L450300, and the FZ250R65KE3 in the transmission-voltage-rated 2L-VSC for parallel wind farm. The on-state and switching characteristics can be found from their datasheets [28]–[30].

Similarly, all diode losses are obtained based a calculation block in Fig. A-2. N_d is the total diode number. R_d and $V_{d.th}$ are the slope resistance and on-state voltage drop. I_d means the diode current. Only the reverse

recovery energy E_{rr} is considered for diode as a function of its current at the turn-off instant, which can be captured using the gate signal of its complementary IGBT module. Fig. A-2 is used to obtain losses for the anti-parallel diodes of all IGBT modules in VSC mode, including 5SNA 2000K452300 (LV side 2L and 3L VSCs), 5SNA 1800E330400 (3L-VSC NPC leg), and FZ250R65KE3 (transmission-voltage-rated 2L-VSC for parallel scheme). Also, this model obtains losses for the fast recovery RB-diode 5SDF 28L4521 in the self-commutated CSC (in series with IGBT).
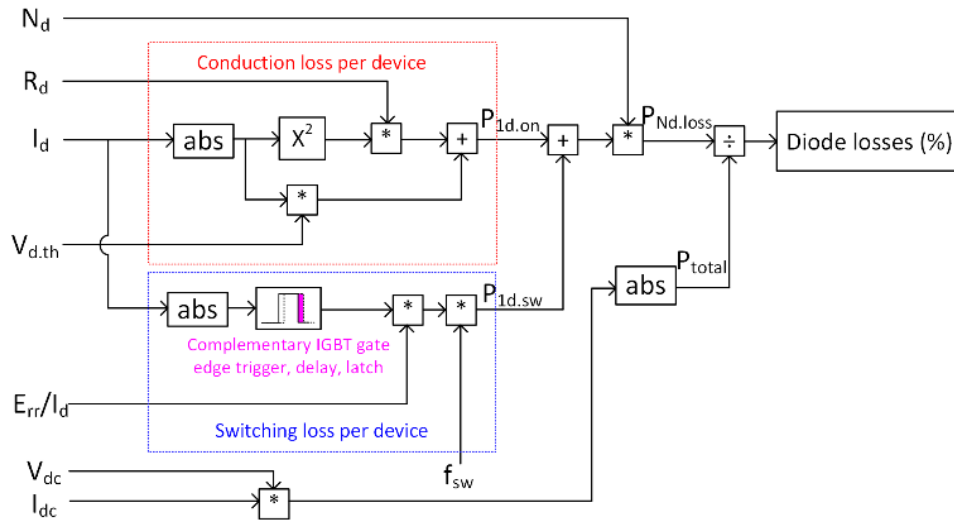

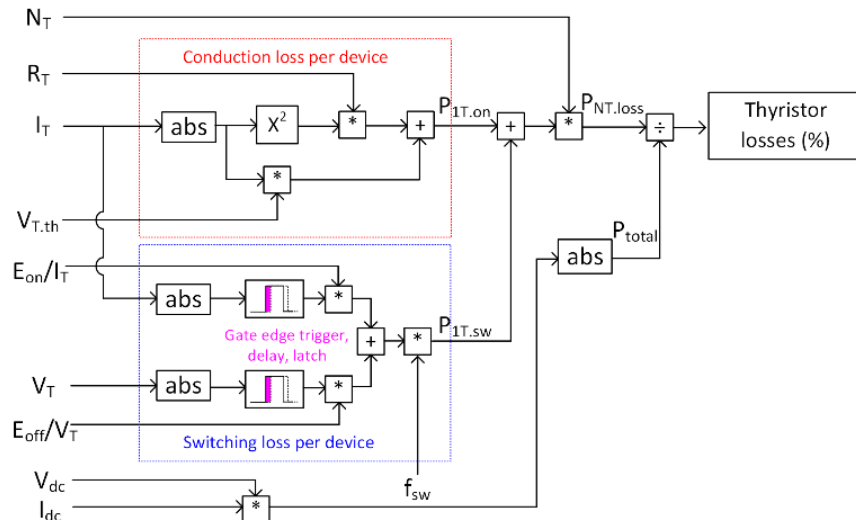Fig. A-2. Online calculation of diode conduction, and reverse recovery losses.

Fig. A-3. Online calculation of thyristor conduction, turn-on, and turn-off losses.

The general loss calculation block for thyristor is shown in Fig. A-3. The mechanism for calculating on-state losses is the same as IGBT and diode, while the turn-on and turn-off energy are obtained as functions

of the current and voltage respectively from the datasheet. Also, the *di/dt* significantly affects the turn-off energy. The reverse recovery charge Q_{rr} is used to estimate the ratio between E_{off} and V_T. Based on the converter design, the CSC *di/dt* can be extracted, and the Q_{rr} for such current commutation rate will be achievable from the Q_{rr} curve in the T2771N datasheet [31].

ACKNOWLEDGMENT

VII. REFERENCE

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