30kW, 200V/900V, thyristor LCL DC/DC converter laboratory prototype design and testing

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***Abstract*-- This paper details design, development and testing of a prototype *30kW*, *200V/900V* resonant *DC/DC* converter. The converter achieves stepping ratio of *4.5* without internal *AC* transformer, and is capable of bidirectional *DC* power flow as well as fast *DC* power reversal. Very importantly, it has capability of *DC* fault isolation on either side, which is of extreme importance for high-power *DC* applications. The design and selection of the individual passive and active components is presented. A *30kW* test setup including one *900V* voltage source converter (*VSC*), one *200V VSC*, and one *200V* current source converter (*CSC*) are designed and built to provide a suitable test rig for prototype *DC/DC* converter. The analytical studies of efficiency are compared with the detailed converter measured efficiency. The prototype shows overall efficiency of around *92%* at full power and weight of around *32kg*, which is promising for scaling to high power applications. The converter operation at full power in step up mode as well as step down mode, and fast power reversal when connected to *CSC* on its low voltage side, are demonstrated by experimental results. Severe pole-to-pole *DC* faults are applied on *900V* and *200V DC* terminals and the inherent *DC* fault isolation capability is confirmed.**

***Index Terms*-- *HVDC* Converters, Resonant Power Conversion, *DC/DC* Power Conversion, Efficiency, *DC* Power Transmission.**

I. Introduction

There is currently a lot of interest in developing medium and high power *DC-DC* converters for applications as diverse as electric vehicles (*20-100 kW*) [1], offshore wind turbines (*3-6 MW*) [2], [3], sub-sea compressors in offshore oil and gas applications (*6-80 MW*) [4], and high voltage *DC* (*HVDC*) applications (*>100 MW*) [5]. Possible technologies include conventional switch-mode type power supplies (generally limited to low stepping ratio) [6], [2], medium-frequency transformer based designs [3], [7-9], and resonant converters [5], [10].

Despite the large number of markets for *DC-DC* converters, no technology has achieved widespread application and there is currently a need for further work both in conceptual design and modeling, as well as in practical testing.

Resonant converters show some promising properties for the high power, high voltage applications as they have low converter weight (with no internal *AC* transformer), high efficiency, can be built with phase control thyristors, capable to link two *VSCs* or one *VSC* to one *CSC*, and have excellent inherent responses to *DC* faults [5].

This article reports on developing a bi-directional *30kW*, *200V/900V*, thyristor *LCL DC/DC* converter with topology given in [10]. The primary goal of the prototype is to confirm the analytically studied converter capabilities by experimental results. We also aim to demonstrate feasibility of scaling up to a *MW* sized unit using the proposed topology of [10], rather than fully optimizing the *30kW* design. Therefore, we will select air-core inductors and phase-control thyristors since these components will be required with MW-size converters. Large *1.8kV/270A* switches are used for *30kW* prototype converter, which are indicative of the technical properties with *MW*-size technologies.

A complete test rig including one *200V VSC*, one *900V VSC* and one *200V CSC* all with *30kW* power rating needs to be designed, developed, and fully tested. The aim is to demonstrate prototype *DC/DC* converter at full power in step up and step down modes linking either *200V VSC* or *200V CSC* to *900V VSC* as well as feeding a high power resistive load from a firm *DC* voltage provided by either *VSCs* or *CSC*. The test rig also requires robust *DC* fault hardware in order to demonstrate very low impedance *DC* faults across the *DC/DC* converter terminals while it is feeding full power in either step up or step down mode.

We will also analyze prototype losses in some depth and in particular, the low voltage side inductors and reverse recovery losses, which cause major design challenges. The thyristors will have large reverse recovery currents and overvoltage spikes at higher operating frequencies and suitable passive *RC* snubbers are required to limit the switch overvoltage spike caused by inductors stored energy at the reverse recovery current snap. The snubber design will be studied in Saber simulator, and tested on the prototype hardware. The converter loss model is developed in Matlab, and the results are compared with detailed measured efficiency obtained in several experimental tests.

Section II of this paper outlines the design of the converter and general component sizes. Section III details the high frequency high power inductor and capacitor design we need for

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resonance circuits. Section IV addresses the laboratory built *DC* grid. The prototype *DC/DC* converter experimental test results are demonstrated and discussed in section V. Section VI shows the converter efficiency analysis.

II. Converter Design

A. Introduction

Figure 1 shows the bi-directional *LCL* thyristor-based high-power *DC/DC* converter described in depth in [10]. Only a summary is given in this section. It consists of two resonant *LC* circuits, back to back connected and sharing a common capacitor C_r in the middle. This topology uses two symmetrical thyristors in each valve and achieves fast power reversal by reversing *DC* currents on high voltage (*HV*) and low voltage (*LV*) side (type II). A unidirectional version would have half the switches [10]. It can also be used for fast bi-directional power flow with current direction change on *HV* side whereas voltage polarity change on its *LV* side in which case *LV* side has half the switches (type I). Type I might be suitable in connecting *CSC* converters (*HVDC* or drives) to a fixed *DC* polarity *DC* grid.

In step up mode, the S_1 and S_2 thyristor pairs are sequentially fired at *50%* duty ratio at f_s switching frequency, which is the converter control input. The inductor L_{LV} creates a resonance with C_r which enables V_{cr} voltage increasing and provides zero-current turn on and off for S_1-S_2.

All the switches should have reverse blocking capability but circuit topology provides current commutation and therefore thyristors are suitable. The high voltage side resonance circuit (L_{HV}-C_r) enables zero current switchings of S_5-S_6 thyristor pairs. In step down mode, the operating principle is similar, but S_3-S_4 and S_7-S_8 thyristor pairs are employed instead (type II). If type I is used in step down then S_1 and S_2 are fired but V_{LV} reverses polarity.

The high voltage circuit is synchronized to operate at same frequency f_s, but there is freedom in choosing firing angle for S_5-S_8 ($\alpha_{step\text{-}up}$ for step up and $\alpha_{step\text{-}down}$ for step down). The high voltage inductors (L_{HV}) are smaller than L_{LV} ones, and less critical for the operation. The converter has the capability of input current inherent reduction in the case of severe *DC* faults on either side [5].

B. 30kW converter design

The design of the converter is based on solving a system of non-linear equations (derived in [10]) to achieve the following specifications:

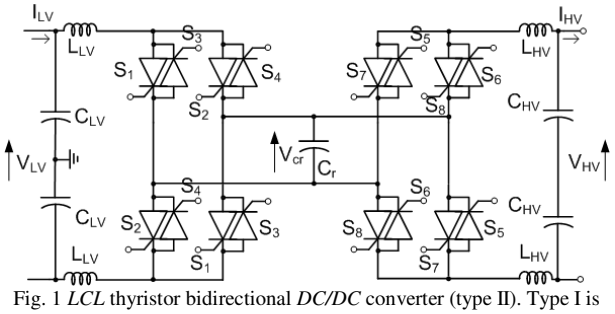


Fig. 1 *LCL* thyristor bidirectional *DC/DC* converter (type II). Type I is obtained if *LV* side thyristors (S_3-S_4) are removed.

1. Maximum power flow of *40 kW* (overrated for control flexibility).
2. Voltage stepping ratio of *4.5* (*200V / 900V*).
3. Maximum peak-to-peak *DC* voltage ripple of *5%*.
4. Provide the minimum switch turn-off time for the selected thyristors.
5. Tolerance for *DC* faults on the *HV* side in step-up mode (tolerance for *DC* faults on *LV* side in step down mode is inherent [5]).

The prototype power and voltage ranges are chosen based on typical ratings for off-the-shelf high-power phase control thyristor modules. Semikron *SKKT 273/18E* (*1.8kV*, *270A*, *150μs*) thyristors for the S_1-S_4 and *SKKT 57/18E* (*1.8kV/50A/80μs*) for S_5-S_8 are used. Note that the switches have higher current ratings to accommodate switching losses.

The converter is only operated in discontinuous mode to provide zero current and controllable *di/dt* at switch turn off. The initial estimates for the component sizes can be obtained using the following simplified equations for the maximum converter power (P_{max}) and switching frequency (f_{smax}) [10]:

$$f_{s\max} \cong \frac{\omega_0}{2\pi} = \frac{1}{4 \cdot T_{off\,\min}} \tag{1}$$

$$P_{\max} \cong \frac{2V_{LV}V_{HV}^2 C_r}{V_{HV} - V_{LV}} 2 f_{s\max} \tag{2}$$

Where, $T_{off,min}$ is the low voltage side thyristor minimum turn-off time (*150 μs*), and

$$\omega_0 = \frac{1}{\sqrt{2L_{LV}C_r}} \tag{3}$$

The turn off time is particularly critical during the faults on *HV* terminal. Using more detailed modelling it can be shown that turn off time also depends on *HV* inductors L_{HV} and firing angle $\alpha_{step\text{-}up}$. Maximising thyristors turn off time will provide additional safety margin for *HV* side *DC* faults and this can be achieved by increasing L_{HV}, or $\alpha_{step\text{-}up}$. However, there is a design trade-off since increasing L_{HV} and $\alpha_{step\text{-}up}$ will lead to higher voltages across the resonant capacitor and could further increase overvoltages during *DC* faults. The converter modelling during *HV* side fault demonstrates that turn off time should meet [5]:

$$T_{off} < \sqrt{L_{LV}C_r}\left(\alpha_{step-up} - \pi\right) + \sqrt{L_{HV}C_r}\,\frac{\pi}{2} \tag{4}$$

The component values are finalized on the model developed on *PSCAD* platform, and the final component sizes and ratings are given in Table I. Note that the *DC* capacitance is oversized for the required maximum *5%* voltage ripple due to component availability at the time of purchase. The components are given for maximum switching frequency of f_s=*580 Hz*.

C. Switching frequency selection

Although (1) gives theoretically maximum switching frequency of *1666Hz* for the *30kW* prototype, a lower nominal frequency is selected to reduce reverse recovery losses.

We have considered two designs: f_s=*1000Hz* and f_s=*580Hz*. Table II compares the components and *LV* side reverse recovery losses ($P_{loss,rr}$) for the two designs, considering ideal lossless *LC* circuit (shown in bracket), and actual *LC* circuit implemented on the prototype. The capacitor size is directly proportional to the power transfer and therefore the internal loss must be compensated by increasing C_r. Using (3), inductor size is calculated for given frequency and capacitance, and it reduces for larger C_r.

From (2) and (3) both C_r and L_{LV} are inversely proportional to the frequency. At higher frequencies, we expect that lower inductor size which implies proportionally lower inductor loss. Nevertheless, the reverse recovery loss increases much faster with the frequency increase as seen in Table II.

Since, the converter is operated in discontinuous mode, zero current turn off is achieved and current derivative is limited by *LC* circuit. At turn off, the current derivative is given by $(V_{HV}+V_{LV})/L_{LV}$, which gives very low values as seen in Table II.

The methodology presented at [11] is employed to calculate peak reverse recovery current from reverse recovery charge obtained from the switch datasheet. It is evident that design at *580Hz* has almost one third the turn off loss at *1000Hz*.

Further analysis has shown that capacitor loss is not significantly increasing with frequency and therefore we have finally selected *580Hz* design.

D. Snubber design

The inductor energy at reverse recovery current snap off causes high overvoltages, which could lead to switch failure. In order to protect the switches, a single *RC* snubber is designed for the four active *LV* side switches (and an additional snubber for *HV* bridge) as shown in Fig. 2. A single snubber design reduces component costs. The snubber parameters are designed based on the methodology presented in [12], and are verified using converter detailed model on Saber platform. The final component sizes are shown in Table III.

While the snubber is effective at reducing overvoltages across the thyristors, the snubber leads to additional losses. Note that:

TABLE I CONVERTER PASSIVE COMPONENTS (F_S=580HZ)

	Size	Component Stress
***LV* Inductor (L_{LV})**	450 µH	500 V_{pk}/175A_{ave}./100A_{rms},1160 Hz
***HV* Inductor (L_{HV})**	224 µH	250V_{pk}/33A_{ave}/37A_{rms},1160 Hz
Resonant Capacitor (C_r)	70 µF	1415 V_{ACpk}/220 A_{rms},580 Hz
***LV DC* Capacitor (C_{LV})**	14100 µF	100 V_{DC}/66A_{rms}
***HV DC* Capacitor (C_{HV})**	470 µF	450 V_{DC}/19 A_{rms}

TABLE II. THEORETICAL REVERSE RECOVERY LOSS FOR TWO DESIGNS

Design	C_r	L_{LV}	$(di/dt)_{off}$	$P_{loss,rr}$
f_s=*1000Hz*	40µF (32µF)	300µH (380µH)	1.8A/µs	478W
f_s=*580Hz*	70µF (56µF)	450µH (650µH)	1.2A/µs	183W

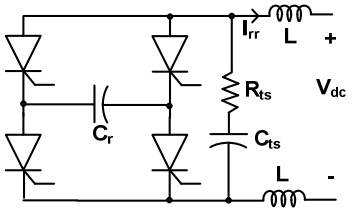


Fig. 2. *RC* snubber circuit.

TABLE III RC SHUNT LV AND HV SNUBBER PARAMETERS

	R_{ts}	C_{ts}
***LV* Snubber**	12 Ω	440 nF
***HV* Snubber**	100 Ω	44 nF

(a) There is a design trade-off between turn-off losses and the switch overvoltage. Reducing the peak overvoltage results in higher losses.

(b) At turn-on of the thyristors the snubber capacitor will discharge into the resonant capacitor leading to higher *di/dt* at turn-on and higher thyristor losses (depending on the size of R_{ts}).

(c) When the thyristors are conducting, the snubber circuit is shunt connected to resonant capacitor C_r, leading to additional losses in the snubber resistor.

(d) On the *HV* side, the turn-off losses will be lower because of the lower *HV* current, and lower reverse recovery charge (smaller switches).

III. HIGH POWER, HIGH FREQUENCY INDUCTORS AND CAPACITOR

The inductors L_{LV} and L_{HV} are the largest components of the converter and will have significant contribution on the converter total losses. In general, high power *DC/DC* converters will require much further development of suitable high power and high frequency inductors. The current in inductors in this topology is *DC* (rectified half-sine) with significant harmonics at $2f_s$, $4f_s$ ... The primary design goal is loss reduction but the weight and size are also considered.

The inductor losses will depend on the harmonics of the input current and the *AC* resistance of the inductor and can be evaluated at different power levels using Parceval's theorem:

$$P_{loss,L} = \sum_f I_1^2(f) R_{AC}(f) \tag{5}$$

Where, the *RMS* current (I_1) at different frequencies can be evaluated by applying the Fourier analysis on the inductor current. The *AC* resistance at different frequencies, $R_{AC}(f)$ increases at higher frequency as the result of skin and proximity effects and very few publications exist on theoretical modeling at high power and high frequency. It is measured on prototype using an impedance analyzer.

Four types of inductors are tested on this prototype *LV* side including: 1) iron core solid-copper *DC* chokes, 2) air core solenoid using stranded copper cable, 3) air core solenoid using stranded tinned copper cable, and 4) air core solenoid litz wire consisting of *135* strands of *0.63mm* wire (final design). The measured *AC* resistance for the above inductors versus frequency is shown in Fig. 3 where the base *DC*

resistance, R_{dc} is around 22mΩ for final design. It is evident that there is very high difference in the *AC* resistance.

The iron core inductors were built externally, but are clearly unsuitable for high frequency operation, because of high losses at higher frequencies as seen in Fig. 3. Note that iron core inductors are also subject to saturation at high currents, which might happen for *DC* faults [5]. The air core solenoid inductors were built in-house using air-core design formulae. The *LV* inductor dimensions as well as its expected losses at full power are shown in Table IV. The designs with stranded copper and stranded tinned copper wire are identical and use same cables, which are generally interchangeable, except that the latter uses tinned strands. We have observed that the tinned cable has considerably higher *AC* resistance, which is caused by current concentration at conductor surface (tin) at higher frequencies. It is also observed that the improvement with the Litz wire inductor over the normal stranded copper is less than might have been expected, in particular at frequency range of interest *500-2000Hz,* since the uninsulated stranded wire offers some benefit at reducing the *AC* losses as discussed in [13].

Note that the values shown in Table IV represents a single inductor in isolation. The individual final inductor is of *320μH,* but we have finally developed two electrically-insulated inductors and closely wound as seen in Fig. 4, in order to increase flux which gives total combined inductance of *900μH* in final design. Observe also that final inductors use densely wound coil (*7x7=49* turns) which gives larger inductance than initial long inductors (*5x14=70* turns).

Two designs for the *HV* inductors (L_{HV}) are used: the first consisting of solid rectangular copper wire wound around an air core, the second using *45* strands of *0.63mm* Litz wire. The dimensions and estimated losses at full power are shown in Table V. Note that because of the higher harmonics (due to a larger gap between current pulses) on the *HV* side current of the converter, there is more improvement when Litz wire is used.

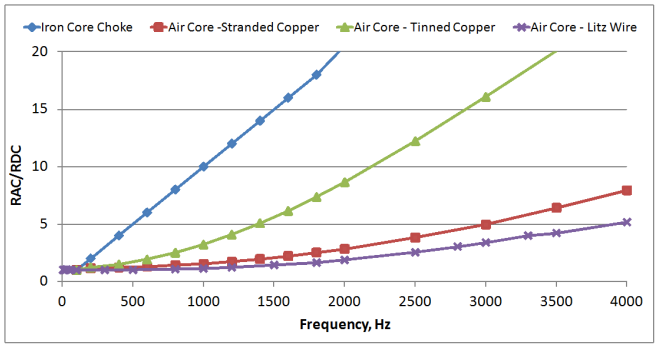


Fig. 3 *LV* inductor normalized *AC* resistance

The resonant capacitor C_r operates at high-frequency (*580Hz* in final design and *1kHz* in initial design), and with main *AC* current but very low harmonics. The current magnitude is directly dependent on the power transfer level. Commonly, the high-power high-frequency capacitors are used in industry only for snubber applications and for induction heating. The selected *AC* capacitor C_r is made of an array of film capacitors with *DC* voltage rating of *1.2kV*, which is derated to maximum *500V RMS* for *AC* voltages.

The capacitor *AC* voltage rating rapidly decreases with frequency increase, but equivalent series resistance (*ESR*) marginally decreases. The array was designed for flexibility in experimenting with different sizes and currently consists of two series blocks of four *30μF* and one *20μF* capacitors in parallel. The datasheet gives maximum dissipation factors of $3x10^{-4}$ for the *20μF* type and $5x10^{-4}$ for the *30μF*. Therefore, the maximum *ESR* of each *20μF*, and *30μF* capacitor would be respectively *4.11m*Ω, and *4.6m*Ω at *580Hz*.

IV. Laboratory Test Platform and DC/DC Converter

A special *DC* test rig including one *200V VSC*, one *900V VSC*, one *200V CSC*, and one *200V/900V LCL* thyristor based resonant *DC/DC* converter all having *30kW* nominal power has been designed, built and tested in the laboratory in order to test *DC/DC* converter in a range of possible applications. On the *LV* side, the *DC/DC* converter can be connected to *200V VSC*, *200V CSC* or *1.3*Ω*/30kW* resistive load (R_{LV}). On the *HV* side, the converter is connected to *900V VSC* emulating a stiff *DC* grid or *26*Ω*/30kW* resistive load (R_{HV}).

The three *30kW AC/DC* converters are built in house and are connected to three-phase *415V* grid voltage via *AC* stepping transformers, in order to provide the required *DC* voltage level. Each one of these high power converters are independently controlled using a *F28335 TI* microcontroller (*150MHz* clock speed, *16* analog inputs, *88* digital *IOs*, and allows floating point arithmetic) and can be run in *DC* voltage or current/power control. An Agilent analogue card is used to provide coordinated *DC* grid control at highest level using LabView program running on one computer.

Each converter is equipped with a range of voltage and current sensors where we use *LEM HAIS* hall-effect based current sensors and *LEM LV 25-P* voltage transducers. Because of *DC* side experimenting, each of these high power converters has overcurrent protection, which trips grid side *AC* contactors in the event of fault. The converters are designed to operate through *DC* faults applied on *DC/DC* converter terminals with no *AC* contactor trip (as no very high current is observed during such fault).

TABLE IV *LV* Inductors Dimensions and Total Expected Losses

	Inductance	Core Dia.	Layers x Turns per Layer	Copper Area	Estimated Losses	Weight
Air Core – stranded copper (initial design, f_s=*1kHz*)	250 μH	115 mm	5 x 14	35 mm^2	2.8%	12 kg
Air Core – stranded and tinned copper (initial design, f_s=*1kHz*)	250 μH	115 mm	5 x 14	35 mm^2	5.2%	12 kg
Air Core -135x 0.63 mm Litz (Final design, f_s=*580Hz*)	320 μH	115 mm	7 x 7	42 mm^2	2%	13 kg

TABLE V *HV* INDUCTORS DIMENSIONS AND TOTAL EXPECTED LOSSES

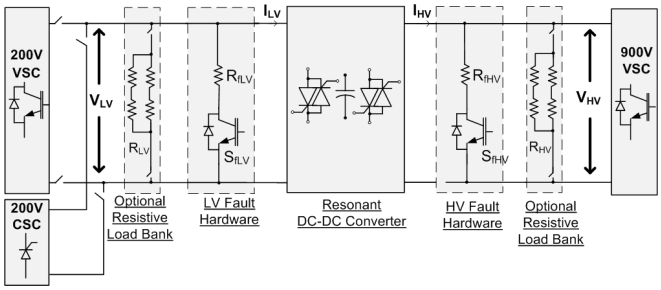
	Inductance	Core Dia.	Layers x Turns per Layer	Copper Area	Estimated Losses	Weight
Air Core – solid copper	220 µH	65 mm	5 x 15	15 mm^2	4%	4.3 kg
Air Core - Litz 45x0.63 mm	220 µH	75 mm	7 x 7	14 mm^2	0.2%	2.8 kg

VSCs employ outer *DC* voltage control loop with independent active and reactive *AC* current inner loops. The switching frequency of *200V VSC* and *900V VSC* is respectively set at *10kHz*, and *1.5kHz*. The *200V VSC* uses higher frequency to reduce *AC* filter size and employs *RCD* snubbers, which protect insulated gate bipolar transistors (*IGBTs*). *LCL* filters are used on *AC* side to reduce harmonics penetrating to the grid.

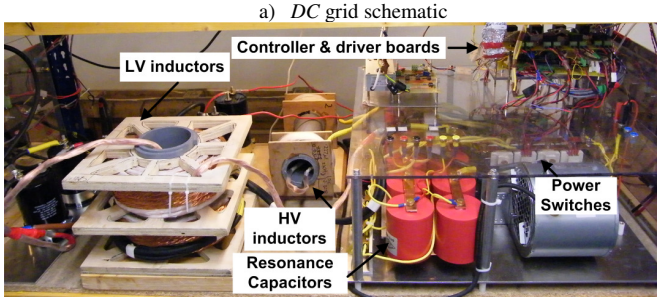
The current source converter also uses *DC* voltage control outer loop with inner *DC* current control loop to provide fault tolerance against *DC* bus short circuit. Minimum extinction angle control loop is also designed to protect the converter in inversion mode against commutation failure. *RC* snubbers are employed across each individual thyristor. Fifth and seventh harmonic filters are placed on the grid side, which will also provide reactive power at grid frequency. Smoothing reactors as well as high pass filters are put on the converter *DC* side.

A simplified *DC* grid schematic as well as photograph of the *DC/DC* converter are shown in Fig. 4.

Two low impedance *DC* fault hardwares have been also designed and built to apply the *DC* fault on either *200V* or *900V DC* bus. A *1.2kV, 683A IGBT* (*SEMiX453GAR12E4s*) in series with small fault impedance (R_{fHV}=*1*Ω on the *HV* side and R_{fLV}=*50m*Ω on *LV* side) is developed. Since transient *DC* faults are studied, a *RC* snubber (*R=20*Ω, *C=220nF*) is used across the *IGBT* to protect the switch at turn off instant.



a) *DC* grid schematic



b) Prototype *DC/DC* converter

Fig. 4. Laboratory built test rig.

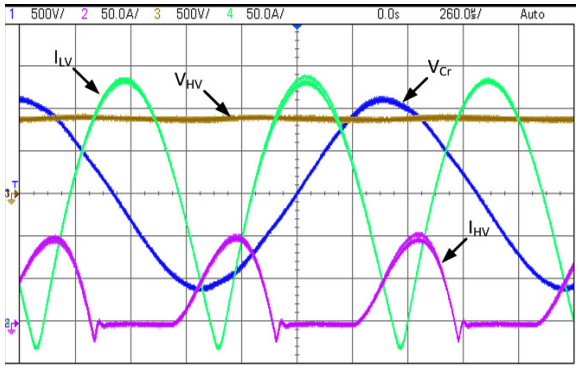


Fig. 5 Steady state test results for step up mode of operation. V_{LV}=*200V*, V_{HV}=*900V*, f_s=*580Hz*. V_{HV}, V_{Cr}: *500V*/div., I_{HV}, I_{LV}: *50A*/div.

V. DC/DC Converter Testing

A. Steady state operation in step up mode

The converter is tested for power export from *200V VSC* or *200V CSC* to *900V VSC*. The test results obtained for *200V VSC* connection to *900V VSC* through *DC/DC* converter at *30kW* output power in step up mode are shown in Fig. 5. It is confirmed that the converter operates close to the border with continuous mode, which gives optimal design. Reverse recovery current on both the *LV* and *HV* thyristors (in particular on the *LV* side) is clearly observed.

Detailed experimental study confirmed the optimum firing angle of $\alpha_{step\text{-}up}$=*130*^{o} for *HV* side thyristors in step up mode in order to maximize *LV* switch turn off time during *HV* side *DC* faults, while minimizing capacitor C_r peak voltage. The resonant capacitor peak voltage reaches to *1.1kV*, which is well below switch and capacitor voltage ratings.

B. Steady-state operation in step down mode

Figure 6 shows the test results in which the *DC/DC* converter is connected to *900V VSC* on its high voltage side and is exporting *30kW* power to a passive low voltage *1.3*Ω resistive load. This figure confirms capability of *DC/DC* converter to drive a passive load, and further tests with active *LV*-side *DC* voltage have been completed. The high voltage side thyristors firing angle in step down mode is set to $\alpha_{step\text{-}down}$=*90*^{o}.

Since a resistive load is employed in this test (and difficulties in obtaining exact resistance at required power), the *HV VSC* is operated at *800V* and the maximum operating frequency has been limited to *500Hz* to avoid *LV* side voltages larger than *220V*. The oscillations on *LV* side current at the switch reverse current snap off are caused by the *RC* snubber in series with L_{LV}. The capacitor peak voltage reaches to about *1.2kV* (generally somewhat higher than in step up operation), which is well tolerated by the selected switches and capacitors.

C. Fast Power reversal

The capability of the *LCL* thyristor *DC/DC* converter in fast power reversal is important in many applications. It is accepted that *HV* side will generally have constant *DC* voltage polarity (*DC* grid), and therefore *DC/DC* converter provides current reversal.

On *LV* side, the *DC/DC* converter can change either current direction or voltage polarity depending on the application. The

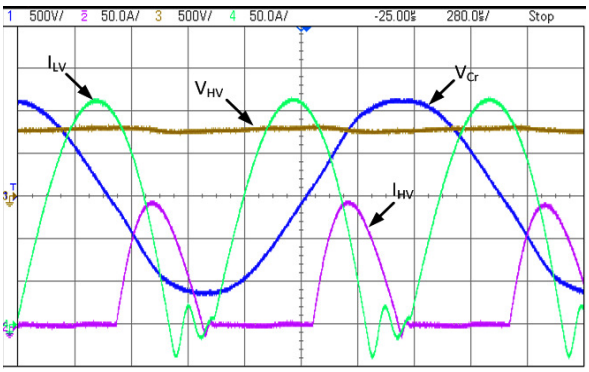


Fig. 6 Steady state test results for step down mode of operation. V_{LV}=*210V*, V_{HV}=*800V*, f_s=*500Hz*. V_{HV}, V_{Cr}: *500V*/div., I_{HV}, I_{LV}: *50A*/div.

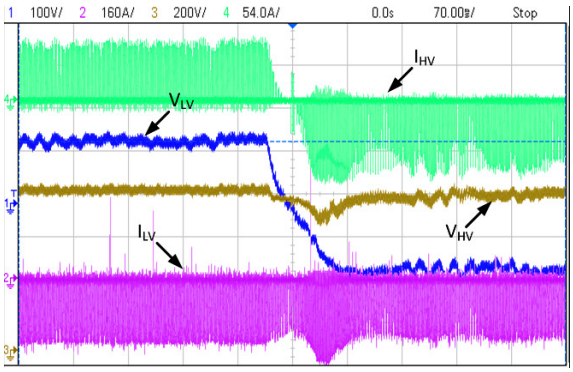


Fig. 7 Power reversal from step up to step down in type I. V_{LV}=*150V*, V_{HV}=*700V*, *P=20kW*. V_{HV}: *200V*/div., V_{LV}: *100V*/div. , I_{HV} :*54A/div.*, I_{LV}: *160A*/div.

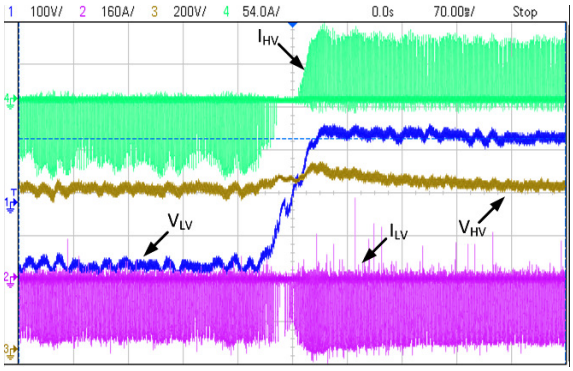


Fig. 8 Power reversal from step down to step up in type I. V_{LV}=*150V*, V_{HV}=*700V*, *P=20kW*. V_{HV}: *200V*/div., V_{LV}: *100V*/div. , I_{HV} :*54A/div.*, I_{LV}: *160A*/div.

topology with current reversal on *LV* side is simpler to design and implement (type II).

In this article, we report on the capability of fast power reversal by changing voltage polarity on *LV* side and current direction on the *HV* side (type I). A typical application would be integration of *CSC* based *DC* systems to *VSC* based *DC* systems. This configuration in fact requires less power electronics on the *DC/DC* converter, but is more challenging, since power reversal on *DC/DC* converter must be synchronized with voltage polarity reversal on *CSC* source (similar as power reversal on thyristor *HVDC* systems).

Figures 7 and 8 show the test results for type I fast power reversal on *30kW* prototype. The results are obtained for *DC/DC* converter linking *200V CSC* to *900V VSC*. Note that the *DC/DC* converter is operated in closed loop with the *LV* side *DC* power regulation. A communication link has been provided between *DC/DC* converter and *CSC*, which is only required to initiate power reversal between the two converters and needs only a digital signal transfer (similar to power reversal process on classic *HVDC)*. The *DC/DC* converter changes its mode of operation as soon as the reference power signal from LabView changes sign. In this instant, the DC/DC converter controller stops triggering *HV* side switches (which are conducting), and initiates firing of the reverse *HV* side switches with different firing angle (Fig. 1). Following power reference signal sign change, the CSC starts changing the DC voltage polarity. Note that a proper sequence of the firing signals must be generated during power reversal to maintain a successful transient. The results show that *HV* side current changes its direction whereas the *LV* side voltage changes its polarity during power reversal, and the whole process takes no longer than *100ms*. A transient voltage drop (or overvoltage) less than *15%* is observed on *HV* side voltage during the fast power reversal. These results also confirm small signal stability and transient performance when a *DC* grid is operated with three large converters (A *VSC*, a *CSC* and a *DC/DC*) with independent feedback controls and through large power swings.

D. DC faults

The *LCL DC/DC* converter offers excellent property of *DC* fault inherent isolation from either side [5]. This is of extreme importance for high power *DC* applications in particular since high power *DC* circuit breakers are not commercially available.

We have applied transient *DC* faults while the converter is feeding a *30kW* resistive load. The converter response to *DC* faults on *HV* side (in step up operation) and *LV* side (in step down operation) are respectively shown in Figs. 9 and 10. Note that the converter is in open loop control (f_s=*580Hz*) in order to demonstrate inherent response, and further control can additionally improve responses. The slow *LV* side voltage drop to zero in figure 10 when the fault is applied is a result of large filter capacitors C_{LV} employed on this side of the converter.

The results confirm that the fault is not propagated to the other side, and the unfaulted side sees load rejection. The converter normally operates through faults and regains its normal power level after the fault is removed. Note that the faulty side *DC* current marginally increases, but is still well within the tolerances of the selected thyristors (this can be improved in closed loop operation).

VI. Efficiency Analysis

Figure 11 shows different losses contribution to the converter total losses obtained from the converter loss model developed in Matlab. The losses are obtained for two different cases of initial design with maximum switching frequency of *1kHz* and the final converter design with f_s =*580Hz*. Using this model, The estimated total loss is *2012W*, and *2345W* for maximum switching frequency of *580Hz*, and *1kHz* respectively.

It is observed that the main sources of losses in this converter include inductor losses (in particular *LV* side inductor loss), and switch losses.

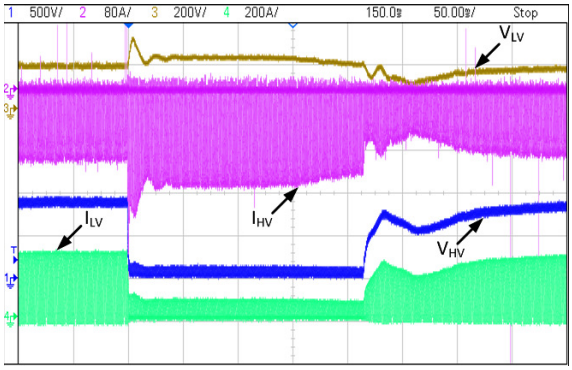


Fig. 9 *HV* side *DC* fault response. V_{LV}=*200V* (from *CSC*), f_s=*580Hz*. V_{HV}: *500V*/div. , V_{LV}: *200V*/div. , I_{HV} :*80A/div.*, I_{LV}: *200A*/div.

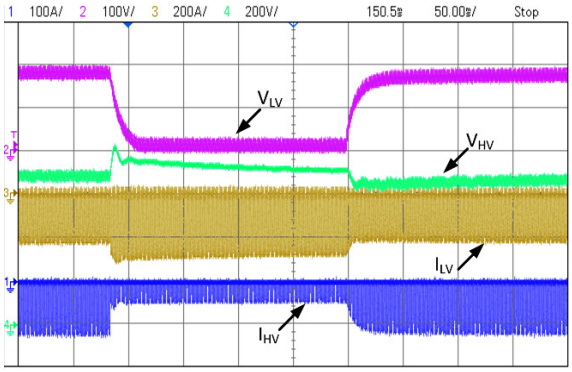


Fig. 10 *LV* side *DC* fault response. V_{HV}=*700V* (from *HV VSC*), f_s=*580Hz*. V_{HV} : *200V*/div. , V_{LV}: *100V*/div. , I_{HV} :*100A/div.*, I_{LV}: *200A*/div.

It is evident that with higher switching frequency, the reverse recovery losses contribution will highly increase but the inductor losses will marginally decrease (smaller inductor is needed). Turn-on losses and off state losses are ignored since the thyristor turn-on transient is very fast and leakage current is quite small.

The converter efficiency is experimentally studied using the test rig. The converter is operated in step-up mode in two scenarios: 1) driving a resistive load and 2) supplying a constant *DC* voltage V_{HV}=*900V* and the efficiency curves are shown in Figs. 12 and 13. . These figures also depict the converter switching frequency versus output power and show the linear variation of output power versus switching frequency when the *HV* side voltage is constant. The converter *HV* side voltage versus switching frequency in step up mode when the converter is connected to *26*Ω resistive load on *HV* side is also shown in Fig. 14. Studying the cases of different V_{LV} in this figure, we can conclude that the converter linearly varies stepping ratio with the frequency input.

The average values of *DC* voltage and current on either side are measured (using voltage and current meters) for power and efficiency calculation. The test is performed for three different *LV* side voltages of *180V*, *200V*, and *220V* in order to analyze impact of stepping ratio. The switching frequency as the converter control variable is varied from *150Hz* to nominal value of *580Hz* in each test.

It is observed that the efficiency marginally decreases while the output power increases. The main reason is reverse recovery losses of the thyristors, which are directly dependent on the switching frequency. In addition, the *AC* resistance of the inductors increases with switching frequency.

It can be presumed that using fast thyristors, which have lower turn-off loses, we could substantially improve efficiency of this design (using higher switching frequency with smaller inductors). However largest fast thyristors are in ratings of *2kV/200A*, and while suitable for *30kW* applications they would not be adequate for higher (MW) powers.

Note that our efficiency calculation is subject to a small error in instruments because of high harmonics and magnetic interference from high current air-core inductors. In addition, the *LV* side inductors have a large thermal resistance, implying different resistance at different tests and difficulties with temperature measurements for internal layers.

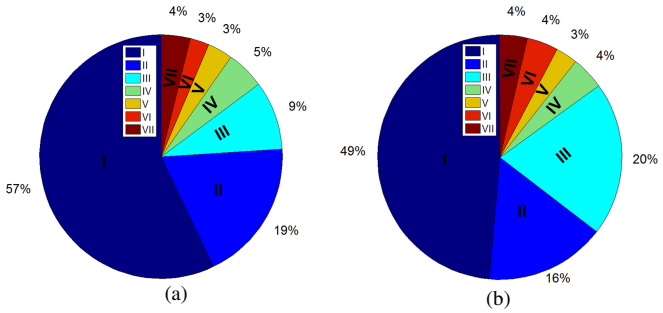


Fig. 11 Prototype theoretical loss study at full power, a) final design with f_{smax}=*580Hz*, Total loss=*2.012kW* b) Initial design with f_{smax}=*1kHz*, Total loss=*2.345kW*. I: *LV* side inductor, II: *LV* side switch conduction, III: *LV* side switch reverse recovery, IV: *HV* side inductor, V: *HV* side switch conduction, VI: *HV* side switch reverse recovery, VII: Resonant capacitor.

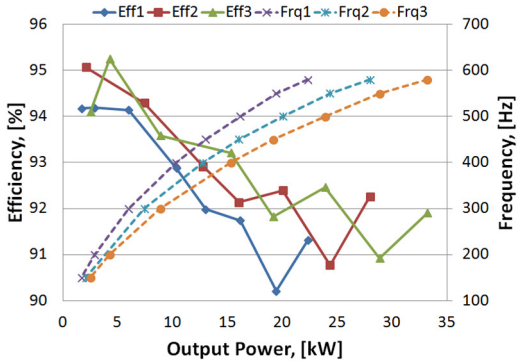


Fig. 12 Measured converter efficiency and converter frequency versus output power in step up mode with resistive load on *HV* side. 1: V_{LV}=*180V*, 2: V_{LV}=*200V*, 3: V_{LV}=*220V*

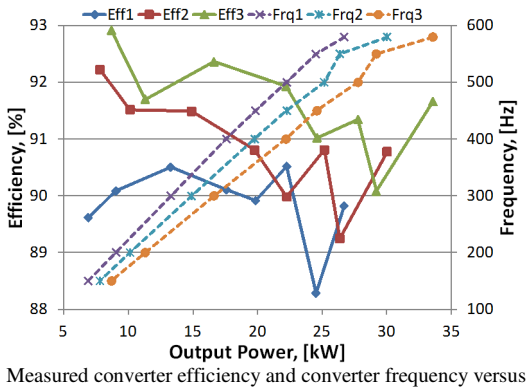


Fig. 13 Measured converter efficiency and converter frequency versus output power in step up mode with firm *900V DC* voltage on *HV* side. 1: V_{LV}=*180V*, 2: V_{LV}=*200V*, 3: V_{LV}=*220V*

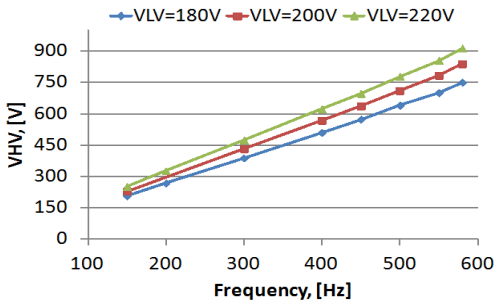


Fig. 14 Measured converter output voltage versus frequency in step up mode with resistive load on *HV* side.

It is evident that for higher *LV* side voltages, higher efficiency is obtained, which is expected as the result of lower *LV* side current magnitude for the same power level. We expect that this topology would give best efficiencies for stepping ratios *2-3* (estimated *96.1%* for stepping ratio of *2*, *200V/400V, 30kW*)..

Comparing the two efficiency results shown in Figs. 12 and 13, it can be seen that the converter efficiency is marginally larger when it is feeding resistive load. When feeding a passive load, the output power is proportional to square of load current, and the load current itself is proportional to switching frequency, and this implies lower switching frequency for a given output power. As the converter output power increases, the resistive load voltage increases and approaches to *900V*, thus closer efficiency results are obtained.

The efficiency of the converter reaches up to *92%* at full power and stepping ratio of *4.5*, which is acceptable for this range of power. The commercialized *20kW DC/DC* converter discussed in [1] shows the efficiency of *96.7%* at full power for stepping ratio of less than *2* (*230V/454V*). Note that more than *50%* of our converter total losses come from *LV* side inductors carrying *175A* average current in full power. This is almost double the current rating of studied Toyota Prius *DC/DC* converter.

VII. Conclusion

A prototype *30kW*, *200V/900V LCL* thyristor based resonant *DC/DC* converter is designed, built and tested. A *30kW DC* test rig including two *VSCs*, and one *CSC* is designed, and built to test the prototype *DC/DC*. The prototype is tested in interfacing either *200V VSC* to *900V VSC* or *200V CSC*, to *900V VSC* or these converters with restive loads. *DC/DC* converter full power test in step up mode, and step down mode, fast power reversal within *100ms* between *900V VSC* and *200V CSC* are demonstrated. The *DC* faults are applied on either side of the prototype and confirm all the predicted fault-isolation properties of this topology. The converter full-power efficiency reaches to up to *92%*, while at partial loading efficiency is better, which are reasonable values for this range of power and voltage stepping ratios. Work is ongoing to further improve the efficiency using fast thyristors, gate turn off thyristors (*GTOs*), or insulated gate commutated thyristors (*IGCTs*) as the converter main switches, to optimize snubber circuits including lossless snubber design, and to improve high power high frequency inductor design.

VIII. Acknowledgement

We would also like to acknowledge significant input from Mr Alan Styles in building this converter.

IX. References

[1] M. Olszewski, “Evaluation of 2004 Toyota Prius hybrid electric drive system”, Oak Ridge National Laboratory, May 2005, pp. 36-39.

[2] W. Chen, A. Huang, C. Li, G. Wang, W. Gu, “Analysis and comparison of medium voltage high power DC/DC converters for offshore wind energy systems”, IEEE Trans. On Power Elec., Vol. 28, No. 4, April 2013.

[3] C. Meyer and R. W. De Doncker, “Design of a Three-Phase Series Resonant Converter for Offshore DC Grids,” presented at the Industry Applications Conference, 2007. 42nd IAS Annual Meeting. Conference Record of the 2007 IEEE, 2007, pp. 216-223.

[4] G. Scheuer et al., “Subsea compact gas compression with high-speed VSDs and very long step-out cables,” in *PCIC Europe, 2009. PCIC EUROPE '09. Conference Record*, 2009, pp. 163-173.

[5] D. Jovcic and B. T. Ooi, “Theoretical aspects of fault isolation on high-power DC lines using resonant DC/DC converters,” *IET Generation, Transmission and Distribution*, p. 8, Sep. 2010.

[6] N. Mohan, T. Undeland, and W. Robbins, *Power Electronics - Converters, Applications, and Design*. John Wiley and Sons, Inc., 2003.

[7] J. Martin, P. Ladoux, B. Chauchat, J. Casarin, and S. Nicolau, “Medium frequency transformer for railway traction: Soft switching converter with high voltage semi-conductors,” presented at the International Symposium on Power Electronics, Electrical Drives, Automation and Motion, 2008, pp. 1180-1185.

[8] H. Akagi, R. Kitada, “Control and design of a modular multilevel cascade BTB system using bidirectional isolated DC/DC converters”, IEEE Trans. On Power Elec., Vol. 26, No. 9, September 2011, pp. 2457-2464.

[9] L. Max and S. Lundberg, “System efficiency of a DC/DC converter-based wind farm,” *Wind Energy*, vol. 11, no. 1, pp. 109-120, 2008.

[10] D. Jovcic, “Bidirectional, High-Power DC Transformer,” *IEEE Trans. Power Del.*, no. 4, pp. 2276-2283, 2009.

[11] Infineon, *Technical Information for Bipolar Semiconductors - Application Note AN2006-03*. 2006.

[12] W. McMurray, “Optimum Snubbers for Power Semiconductors”, *IEEE Trans. Ind. Appl.*, vol. 8, no. 5, pp. 593-600, 1972.

[13] Xu Tang and C. R. Sullivan, “Optimization of stranded-wire windings and comparison with litz wire on the basis of cost and loss,” in *Power Electronics Specialists Conference*, 2004.

X. Biographies

Masood Hajian (M'10) received the B.Sc. degree from Sharif University of Technology, Tehran, Iran, and the M.Sc. and Ph.D. degrees from Isfahan University of Technology, Isfahan, Iran. He was a visiting researcher in Laboratory for Electric Drive Applications and Research (LEDAR), Toronto, from April 2010 to February 2011. He is currently a lecturer at University of Aberdeen, Aberdeen, U.K. His main research interests include power electronics, electrical machines, nonlinear control, and variable speed electrical drives.

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Dr. Wu received the Gold Medal of the Governor General of Canada, the Premier's Research Excellence Award, Ryerson Distinguished Scholar Award, Ryerson Research Chair Award and the NSERC Synergy Award for Innovation. He is a fellow of Engineering Institute of Canada (EIC) and Canadian Academy of Engineering (CAE). Dr. Wu is an Associate Editor of IEEE Transactions on Power Electronics and IEEE Canadian Review.