Experimental Evaluation of 5 kV, 2 kA, DC Circuit Breaker with Parallel Capacitor

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Abstract— **This article describes design, operation and experimental testing of a mechanical DC CB (Circuit Breaker) with parallel capacitors. The topology resembles hybrid DC CB but there are possible advantages in the costs since the main semiconductor valve is replaced with capacitors, and in performance since this breaker inserts counter voltage earlier. A detailed PSCAD model is employed to support DC CB design and to analyse operating principles. A 5 kV, 2 kA hardware demonstrator with 1.5 ms disconnector opening time is developed in the university laboratory. The test results demonstrate successful breaking of DC currents, with the measured time for insertion of capacitor voltage of around 290 µs. Further experimental analysis evaluates stresses on the key components, optimal timing for opening of LCS (Load Commutation Switch) and the margins for successful current interruption.**

***Index Terms*-- DC switchgear, HVDC protection, DC Circuit Breakers.**

I. Introduction

There is significant interest worldwide on developing high voltage direct current (HVDC) transmission grids [1], and the first DC grid has been implemented in China recently (Zhangbei project) [2]. DC CB (Circuit Breakers), as key components in DC grids, have been in rapid development in the past 10 years. There are many different DC CB topologies, and a good overview is provided in [3][4], which also recommend grouping of DC CBs in two families: hybrid and mechanical. In general, faster DC CBs bring significant advantage since peak fault current becomes lower, DC system restoration is faster and there is less chance of blocking/tripping converter stations.

Hybrid DC CBs operate quite fast, within 2-3 ms, but they include a high-voltage semiconductor valve [5][6][7] which significantly increases breaker cost. They have been commercialized to high voltages and implemented in the Chinese DC grid and in the multiterminal Zhoushan HVDC.

Mechanical DC CBs use electromechanical components [8] and perhaps some low-rated semiconductor valves [9], but generally have slower opening speed, of around 8-10 ms. The recent installation in Zhangbei DC grid achieves faster 3 ms operation [10], although the basic modules have 50 kV rating.

It is recognized that in addition to operating speed and peak fault current, the cost of the existing DC CB is high and is one of the impediments for further DC grid development.

Recently, a new DC CB topology based on parallel capacitor has been investigated [11], and results show potential benefits in terms of performance and costs. A similar concept using solely mechanical components is called LC DC CB and has been demonstrated on hardware at 130 A, 1.3 kV in [12], while laboratory demonstration in [13] provides 400 A, 1.3 kV demonstration. Compared with the hybrid DC CB, the topology with parallel capacitor potentially offers the following key advantages:

- High voltage semiconductor valve is eliminated,
- The current commutation occurs at the beginning of disconnector switch stroke, thus inserting counter voltage earlier and lowering peak fault current.

A major challenge with early commutation is limiting of voltage stress across moving contacts. The voltage stress control across moving contacts of disconnector has been investigated in [14], but pulse-width control of semiconductors is employed which would be costly with high-voltage systems. Passive voltage control using capacitor is demonstrated on hardware in [12] and [13] but only at low voltages.

The primary challenge with parallel capacitor-based topologies is the current commutation into capacitor. Internal DC current commutation (between DC CB branches) is a peculiar challenge with all DC CBs, and multiple options exist as elaborated in depth in [15]. All the commercialized DC CB topologies commutate DC current at the end of stroke of the mechanical switch. The commutation at the beginning of contact stroke has been demonstrated experimentally only at low currents in [13].

With fast hybrid breakers the current is commutated using semiconductor-based LCS (Load Commutation Switch). As an alternative, recent research demonstrates experimentally successful high DC current commutation directly using fast disconnectors [16]. However, commutation occurs in a parallel closed circuit, while arcing may take tens of ms and reignition may occur making such commutation uncertain.

Fast disconnectors are of special interest as mechanical switches in DC CBs since they have the fastest opening speed and have been commercialized for high voltage [17], even though they have no capability to sustain arcing. Therefore commutation method without arcing is preferred.

This project will advance further parallel capacitor topology and investigate DC current commutation into a capacitor using

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semiconductor LCS. We will describe design of a 5 kV, 2 kA hardware DC CB in University laboratory, and provide test results. Simulation model will be employed to provide theoretical analysis, and to support hardware design.

Section II lays out the main hypotheses of the proposed DC CB. Section III analyses the operating principles using PSCAD simulations. Section IV describes the details of the laboratory test system. Section V presents experimental results.

II. Topology and Hypothesis

A. Circuit description

Fig. 1 shows the topology of DC CB under investigation. It consists of the following main components:

- S_1 is UFD (ultrafast disconnector), similar as in [5] and [17]. It is desired to have fast opening and negligible arcing. This switch should have contacts with lateral overlap to enable high speed at separation, and in our study disconnector with air insulation is used [12].
- T_1 is a load commutation switch as in [5]. It should be rated for load current, but for low voltage. It is implemented as a matrix of several series-parallel transistors, capable of opening in few µs [18].
- SA_{T1} is arrester which limits voltage across T_1.
- C_{T1} is snubber capacitor.
- C_s is parallel capacitor, similar as in [12][13]. It is rated for the arrester bank SA voltage.
- SA is energy absorber (bank of arresters) similar as in [5]. It is rated for somewhat higher nominal DC voltage.
- S_2 is a residual switch. This is normally a standard single-phase AC Circuit breaker.
- L_{dc} is required to limit the slope of current.

When the trip signal is received, S_1 is commanded to open immediately. Opening of LCS should occur around the time when contacts of S_1 begin to separate. LCS provides adequate counter voltage to commutate current in C_s, while the rate of capacitor C_s voltage rise is proportional to the current and the capacitance C_s. The main advantages of the circuit are:

1) Compared with hybrid breaker, the main semiconductor valve is replaced with a capacitor C_s, and this brings cost benefits.
2) The voltage rise across disconnector S_1 is limited by capacitor Cs. This means that the commutation to the capacitor could be achieved at the beginning of the disconnector contact stroke, leading to earlier insertion of counter voltage. With hybrid DC CB [5], commutation occurs at the end of the stroke, i.e 2 ms after the trip signal.

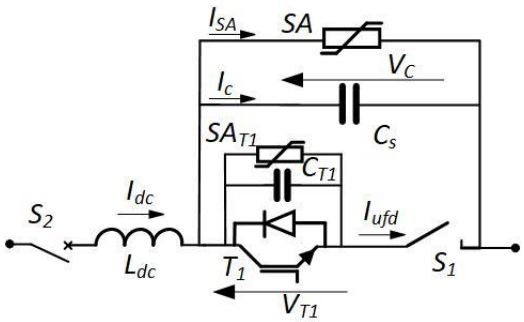

Fig. 1 DC CB with parallel capacitor.

B. Hypothesis and design challenges

The primary design challenges include:

- Determining optimal timing for T_1 opening.
- Determining voltage stress on T_1.
- Understanding voltage sharing between T_1 and UFD, and determining safety margin for full voltage sharing by UFD after commutation.
- Understanding voltage stress on UFD for full contact stroke, under various operating conditions.

III. Circuit Analysis using PSCAD Model

A. Test system design

The design aim is 2 kA interruption at 5 kV DC voltage. The design follows the basic principles for LC DC CB as described in [12]. For the given commutating current I_0=2 kA, contact velocity at separation v_0=5 m/s (as described in Section IV. C.), and dielectric strength for air d_{air}=3 kV/mm, the minimal capacitor C_s can be determined as [12]:

$$v_0 d_{air} > I_0/C_s \quad (1)$$

This gives capacitance of C_s>133µF. Assuming no parasitics in the circuit, this capacitor value would ensure current commutation without T_1 [12]. Since parasitics inductances are present in C_s and in the commutating circuit, it is necessary to build commutating voltage to enable current commutation. The arc-driven commutating voltage enabled commutation of 400 A in [13], where the parasitic inductances were modest because of low voltage components (1.3 kV). It is noted that non-zero contact speed at separation is essential, and therefore contact overlap is needed (but contact design is not suitable).

In this study we use LCS to achieve the required commutating voltage. The design of LCS for hybrid breaker is analysed in [18], but the DC current is commutated in a parallel closed circuit, rather than a capacitor.

B. PSCAD DC CB Model

Fig. 2 shows the schematic of the detailed model developed in PSCAD with numerical values for all parameters. All the component values from the hardware set up are used. The parameters of the parasitics are calculated using theoretical model (arresters, IGBT) or measured on the test circuit (cables, capacitors) and then fine-tuned to enable matching of the model with the hardware responses. Transistor is an ideal switch with ON/OFF resistances according to manufacturer's data.

Capacitor C_s=400 µF is selected larger than the value in (1) because of uncertainty with d_{air} caused by dielectric ionization, and to provide some safety margin.

The model for disconnector is described in [19], and includes detailed dynamic trajectory of the contacts based on kinetics of contacts and electro-dynamic model of Thomson coil actuators. It includes dynamic dielectric stress and arc model (in air).

C. Illustration of operation and T_1 timing analysis

Fig. 3 illustrates PSCAD model responses with successful DC CB breaking assuming that T_1 opens exactly when contacts separate. It is concluded that the breaking is successful since I_{UFD} drops to zero and capacitor C_s takes full fault current. Fig.

4 shows unsuccessful DC CB opening (I_{UFD} drops to zero but then returns to high value) because of too early T_1 opening.

The following timing notation is used:

- t_0 – fault instance.
- t_{UFD} – trip signal to UFD (S_1). Contacts begin to slide.
- t_c – UFD contact separation. UFD has overlapping contacts which slide in the interval t_{UFD} to t_c.
- t_{T1} – Opening of T_1.
- t_e – UFD arc interrupted and UFD takes voltage stress.
- t_w – Voltage V_c equals arrester SA_{T1} saturation voltage. At this instant UFD takes full voltage stress.

The curve labeled V_{UFD_max} is the maximum UFD voltage for the instantaneous contact separation distance x, obtained as:

$$V_{UFD\_max} = xd_{air} \quad (2)$$

The dielectric breakdown occurs if $V_{UFD} > V_{UFD\_max}$, and adequate safety margin is required for the full travel of contacts. The curve V_{UFD_max} is nonlinear because of the dynamics of the UFD contact movement, while V_{UFD} curve has different nonlinear shape caused by the dynamics of the current circuit.

The arcing starts at t_c, when contacts separate. In the model in [19] the exit from arcing (time t_e) occurs when the following two conditions are met:

1) The dielectric strength is adequate ($V_{UFDmax} > V_c - V_{T1}$) This occurs after t_c and is largely dependent on the distance between contacts.
2) The current is below chopping value (set to 1 A). This occurs sometime after T_1 opens (t_{T1}). Therefore t_e occurs:

$$t_e > \max(t_{T1}, t_c) \quad (3)$$

In practice, the success of interruption will further depend on the derivative of voltage and current but also on the thermal phenomena which influence dielectric strength (d_{air}).

UFD shares V_c voltage stress with T_1. In the case of successful breaking in Fig. 3, it is seen that UFD takes full voltage stress at the instant t_e, when V_{T1} and V_c curves separate, indicating that contacts have separated and arc is interrupted.

The time instant t_e cannot be predicted exactly but it is usually 20-70 μs after the larger value of t_c, and t_{T1} and it depends primarily on the current level at commutation as it will be shown with the experimental results. Opening T_1 at t_{T1} UFD current will drop to zero shortly but there will be oscillations on both V_{T1} and I_{UFD} because of parasitics. It is seen in Fig. 3 that t_e can be approximated with the time when parasitic oscillations significantly reduce.

The case of unsuccessful breaking in Fig. 4, is shown to enable study of the margin for successful breaking. This figure reveals the time instant t_w, when the voltage V_c reaches the value of saturation voltage of arresters SA_{T1}, and current commutates back from capacitors to arresters SA_{T1} and UFD.

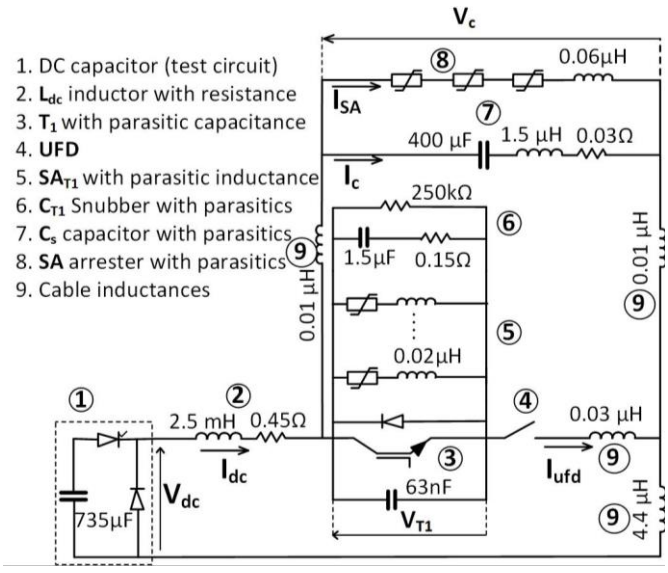

Fig. 2 Schematic of pscad model (with parasitic parameters)

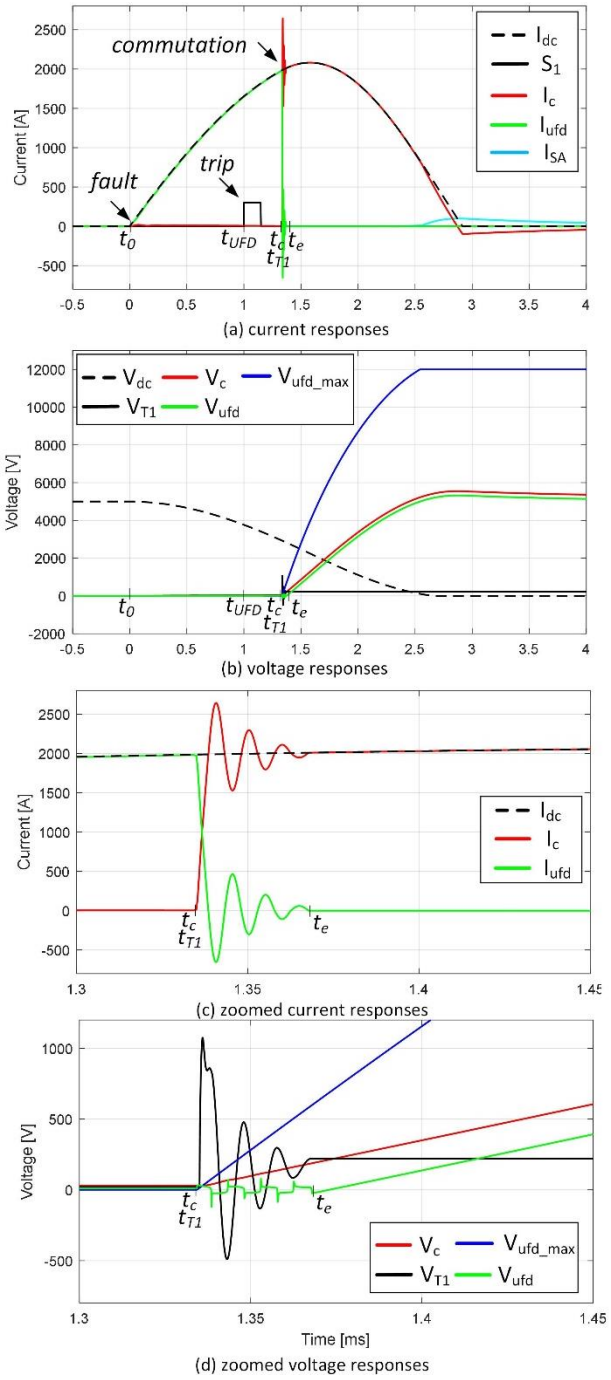

Fig. 3 PSCAD model simulation of successful breaking of 2kA current.

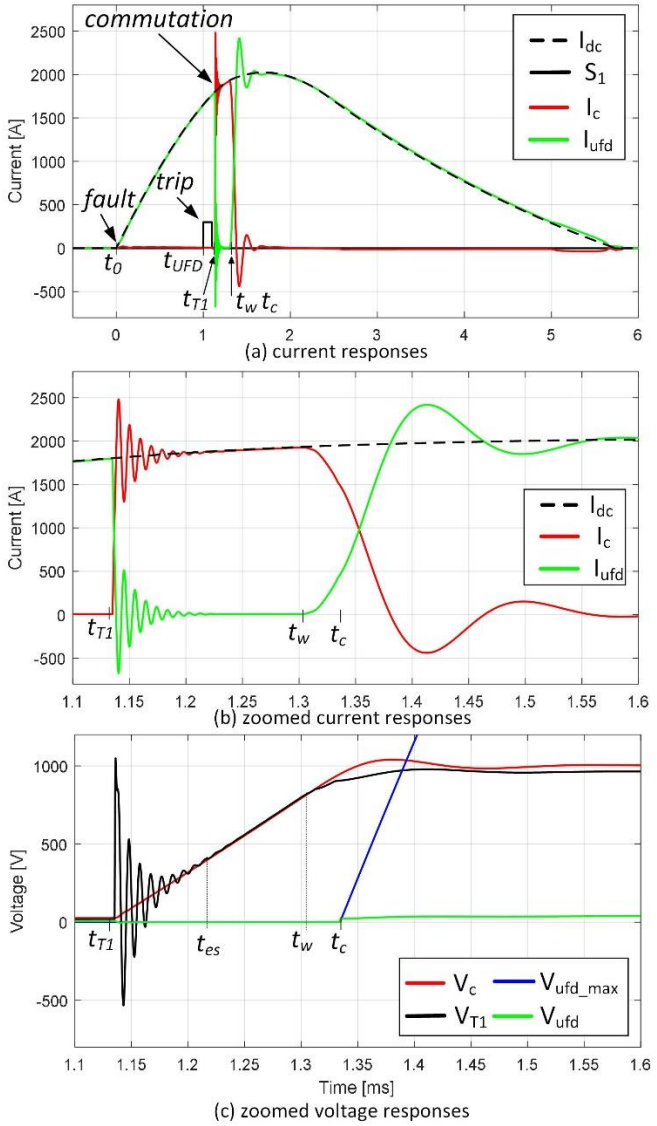

Fig. 4 PSCAD model simulation of unsuccessful breaking of 2kA current, because of too early opening of T_1.

Therefore, it is necessary that the arc interruption should occur before t_w for successful breaker operation:

$$t_e < t_w \tag{4}$$

The time t_w can be estimated by knowing t_{T1}, the arrester saturation voltage and the voltage gradient (I_o/C_s). In Fig. 4. time t_{es} defines extinguishing of oscillations, and it can be approximated with t_e (had t_c occurred timely). It is concluded that in our design the time window for successful opening is around t_w-t_{es} ≈100 µs.

In practice, t_c will be known from the disconnector design, which remains constant for all current magnitudes (it may vary because of contact wearing and free play). This enables designers to determine t_{T1} and to estimate the margin.

If T_1 opens too early as seen in Fig. 4, then the contact separation time t_c occurs after t_w, and conditions (3) and (4) are not met. UFD current drops to zero (current is commutated to C_s) but then it increases again at t_w. Since contacts have not separated by this time current continues to flow through UFD.

The case when T_1 opens too late will induce prolonged arcing in the time period t_e-t_c. This arcing causes ionized bridge between contacts and possibly thermal damage on the contacts. Such case may or may not lead to successful breaking, but this situation cannot be simulated well on PSCAD since thermal arcing phenomena are extremely difficult for modelling.

IV. Hardware Test System Description

A. 5.2 kV, 2 kA DC CB test circuit

Fig. 5 shows the schematic of the 5.2 kV DC CB testing circuit, which is an upgraded version of the circuit in [13]. The input AC voltage is adjusted by the variac between 0 and 260 V and this is boosted by step up transformer up to single-phase 4 kV AC. The diode bridge D_1-D_4 is used to rectify the stepped-up voltage, which provide up to 5.2 kV DC voltage.

The capacitor charging current is limited by resistor R_c=22 Ω and R_r=10 Ω. The charging is initiated by closing S_1, and later S_2 closes and bypasses R_c. Once the capacitor bank is charged, the charging circuit is disconnected by the opening of S_1 and S_2. Capacitor C_b is implemented as a 5x4 matrix of 590 µF capacitors with a cumulative capacitance of C_b=737.5 µF. The

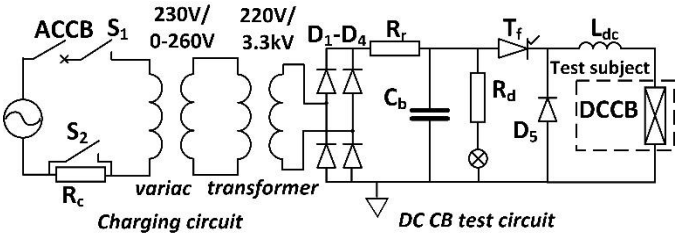

Fig. 5 Schematic of the DC CB test system.

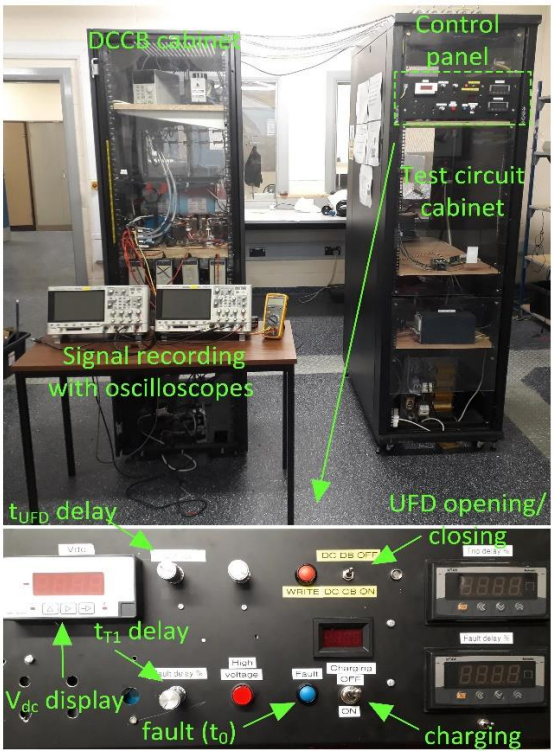

Fig. 6 Cabinets with DCCB and test circuit.

maximum energy is 9.97 kJ. The fault is initiated by firing T_f thyristor. The current rise time can be regulated by changing the value of the inductor L_{dc} (2.5 mH is chosen for this set-up). When the capacitor voltage reaches zero, D_5 takes the current flowing through the DC CB (unless it was already interrupted). T_f turns off naturally when D_5 takes the current.

The resistor R_d=500 kΩ, provides safe discharge while LED light is installed in series with R_d to indicate the state-of-charge of the capacitor. The DC CB and the test circuit are located in separate cabinets which are shown in the photograph in Fig. 6.

The test circuit cabinet has a control panel which controls charging and discharging (t_0) and also to provides settings for the DC CB trip delay (t_{UFD}) and T_1 turn off delay (t_{T1}).

B. 5 kV, 2 kA DC CB

Fig. 7 shows the photograph of the DC CB lab set-up which is made in-house. The current clamps show the position for measurement of experimental signals. The 20 mm bus bars are used to reduce parasitic impedance in the main commutation path. The list of all key components is provided in TABLE 1.

Arresters SA are selected to clip V_C to around 5.5 kV and the energy rating has been calculated using PSCAD model. Three different values for SA_{T1} arresters are used to analyse T_1 stress, with saturation voltage 350 V, 600 V, and 900 V. They take commutating current for only around 10 µs, but in a case of unsuccessful breaking (UFD arcing) they will take full fault energy. The transistor T_1 is rated for 1.5 kA,1.7 kV and it can interrupt 3 kA peak current. The Infineon IGBT module has two transistors, but only one is used in our circuit.

C. 6.5kV, Ultrafast disconnector

Fig. 8 shows photograph of Ultrafast Disconnector, which is fully made in house. It employs two moving contacts, each driven by 2 TC (Thomson Coil) actuators. It is based on the design described in [12], but the opening speed and the separation distance have been increased. Dynamic damping is introduced to reduce bounce at the end of the stroke.

Fig. 9 shows photograph of the contact assembly. There are 2 break points, however in this study only one break point is utilized. The upper single contact is firmly fixed to the holder, while the lower 2 contacts are on springs to provide adequate force on the contact surface in the closed state. The lower 2 contacts are approximately 20 mm x 10 mm, and there is around 4 mm overlap with the fixed contact in the closed state. Therefore, we have around 80 mm^2 contact surface in the closed state, although we have not tested contacts for prolonged continuous current in the closed state. Fig. 9b) shows the set of contacts after arcing caused by unsuccessful breaking. Copper contact material is selected for convenience of manufacturing.

TABLE 1 List of DC CB components with parameters

Capacitor C_s	400 µF, 6.5 kV, Cornell Dublier (10 kA current)
IGBT T_1	1.5 kA, 1.7 kV, Infineon FF1500R17IP5BPSA1
Snubber C_{T1}	1.5 µF, 2 kV
Arresters SA_{T1}	Parallel 3 x EPCOS B60 K385 (1 kA,0.9 kV), or parallel 3 x EPCOS B60 K230 (1 kA,0.6 kV), or parallel 3 x EPCOS B60 K150 (1 kA,0.35 kV),
UFD	In house made, single breaking point, 1.5ms opening time
Arrester SA_{Cs}	Series EPCOS B60 K550, B60 K150 and V172 BB60 (1 kA, 5.5 kV). Total energy is 8kJ (2ms).

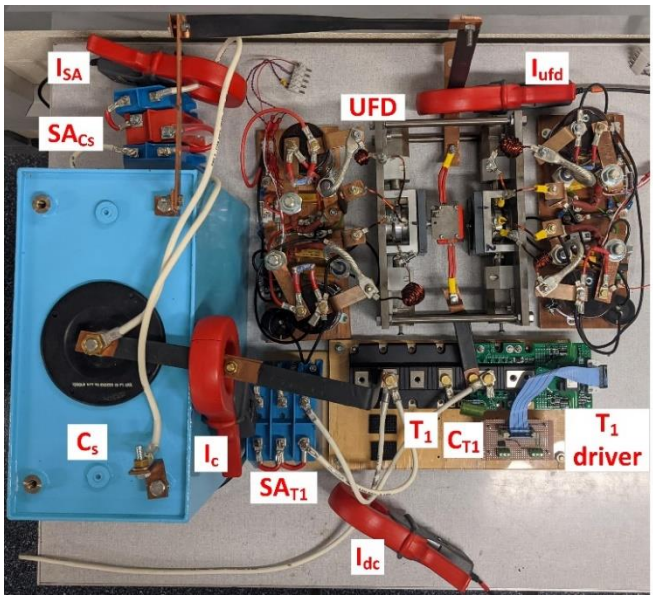

Fig. 7 Photograph of 5 kV, 2 kA DC CB with parallel capacitor.

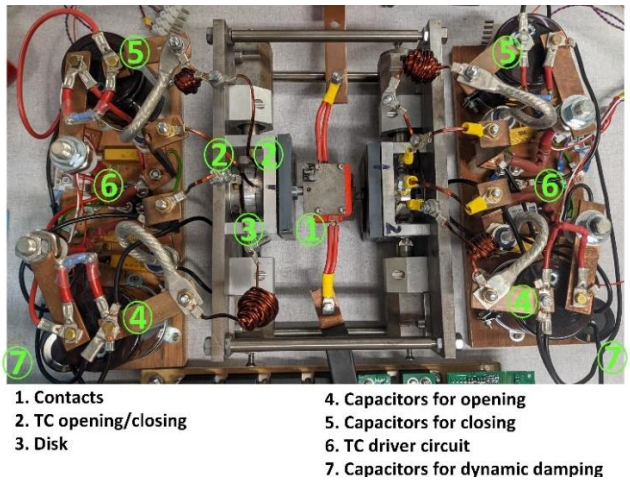

Fig. 8 Photograph of Ultrafast Disconnector (1.5 ms opening time).

These contacts cannot sustain arc and contact replacement is required after each unsuccessful breaking. With successful DC current breaking arcing is extremely short and no visible damage occurs. Two cables connect to each contact to reduce impedance.

Fig. 10 shows the experimental measurements of the UFD contact position. Hall-effect sensors are used as described in [12], and it is seen that there is some difference between the stroke of the two contacts. The full separation distance is around 4 mm (giving theoretical maximum stress of 12 kV) and it is achieved in around 1.5 ms. The velocity of contact separation is 5 m/s at the separation instant and then gradually reduces because of the damping pulse and friction. It is seen that the PSCAD model represents contact dynamics very well.

The instant of UFD contact separation t_c is determined experimentally. We used the same DC CB but kept LCS closed which converts this breaker into LC breaker as described in [12]. LC breaker is capable of interrupting low current and Fig. 10c) shows 10 A breaking at t_c≈290 µs. Subsequent tests have confirmed that t_c remains consistent (independent of fault current) although small variations within ±10 µs occurred.

These variations are caused by the inaccuracies in contact geometry and some free play in the contact assembly.

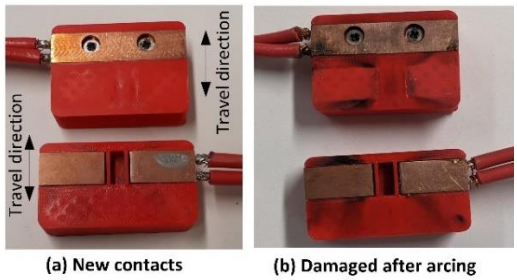

Fig. 9 Photograph of UFD contacts: (a) new contacts (b) arc damage

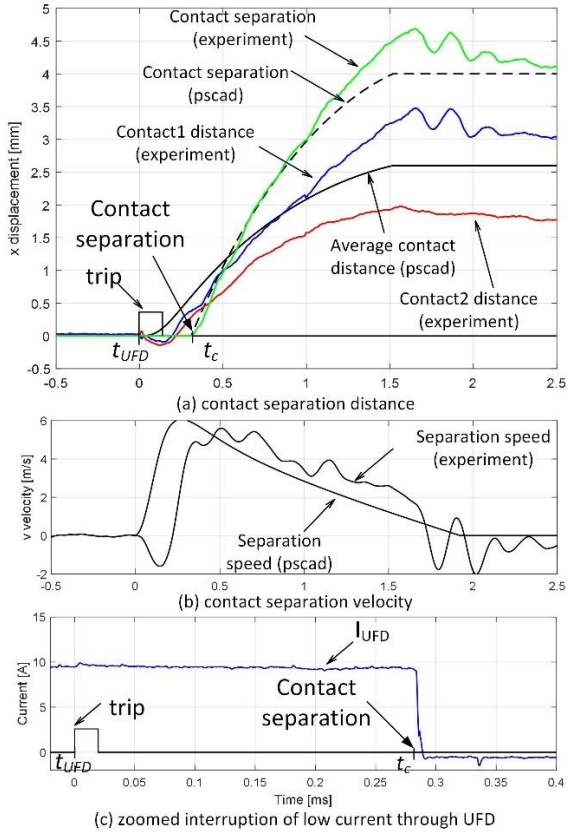

Fig. 10 UFD contact position measurements, and PSCAD model results.

V. DC CB Experimental Results

A. Commutation with closed UFD contacts

Firstly, we performed tests with UFD kept closed, which enables identifying timings and to verify stresses on the LCS.

Fig. 11 and Fig. 12 show the DC CB current commutation with closed UFD contacts. Two sets of SA_{T1} arresters are considered: K385 which saturates at around 900 V in Fig. 11, and K150 which saturates at around 350 V in Fig. 12. These figures enable determining time interval between t_{T1} and t_w. The time t_{T1} is not the same as the timing which is programmed in the microcontroller for T_1 turn off, since there are delays in the transistor driver and T_1 turn off (around 100 µs). Also, it is seen that T_1 turn off transient takes around 10 µs.

It can be observed that the UFD current remains zero for a period of around 50 µs with K150 arresters and around 130 µs for K385 arresters. This gives wider margin for setting timing t_{T1} with higher-voltage K385 arresters. Similarly, at lower currents this margin becomes wider. However, this gives only the initial (optimistic) margin. The actual value for margin is narrower, since it depends on time t_e, which will be determined with DC CB tests in the Section V. B.

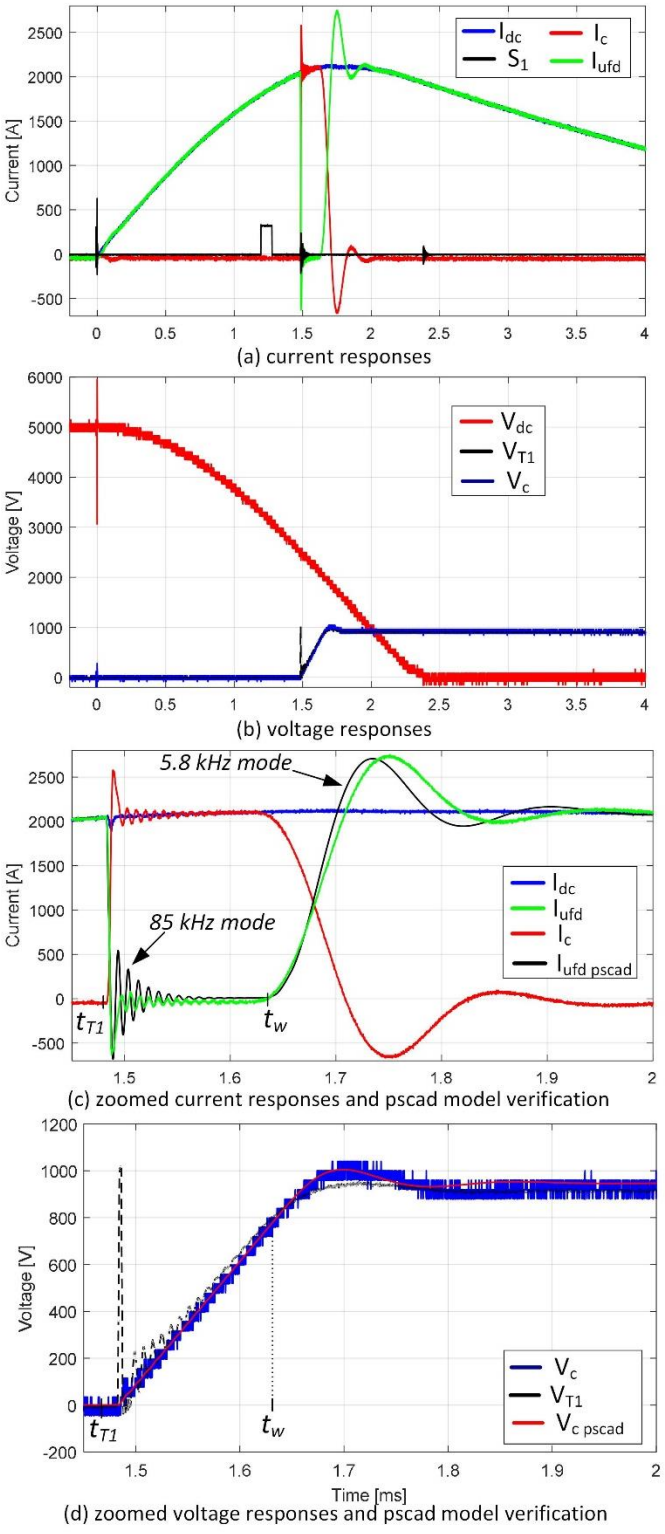

Fig. 11 Experimental results of 2kA DC current commutation with closed UFD ($K385\ SA_{T1}$ arresters).

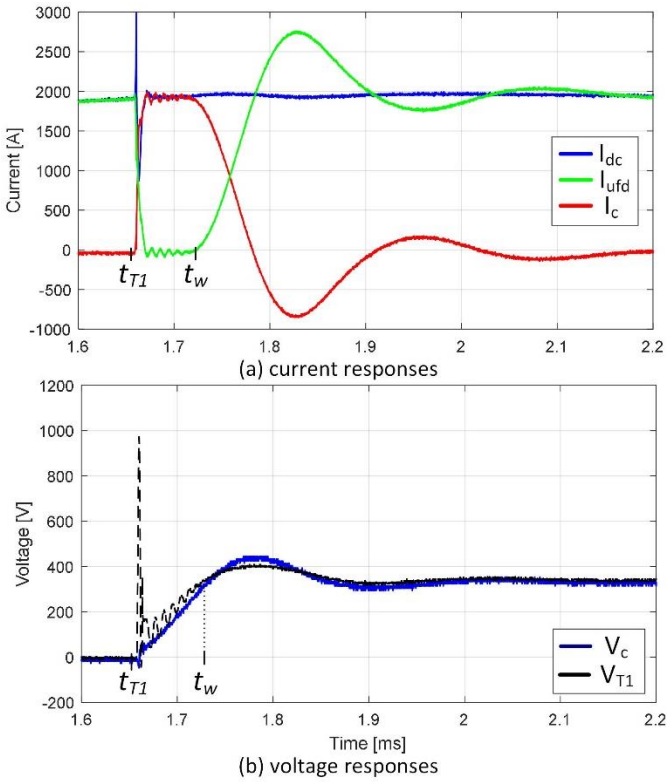

Fig. 12 Experimental results of 2kA DC current commutation with closed UFD (K150 SA_{T1} arresters).

Although we have been able to break quite high current of 1.7 kA with lower-voltage K150 arresters, the accurate timing of T_1 becomes challenging with these arresters. Most further tests were therefore performed with K385 SA_{T1} arresters.

These figures also show that there is a substantial difference between transistor voltage V_{T1} and capacitor voltage V_c in the first few µs after T_1 opening. V_{T1} peaks to almost 1 kV (it is same value in Fig. 11 and Fig. 12) because of parasitics between LCS assembly and C_s. This indicates that SA_{T1} is ineffective in protecting transistor under fast transients. For this reason, snubber C_{T1} is introduced which limits transient transistor stress to approximately the saturation value of K385 arrester.

The last two graphs in Fig. 11 show also PSCAD model verification. The PSCAD model matches very well the dominant oscillatory mode at around 5.8 kHz caused by the parasitics in the main commutation path and which determine the arrester SA_{T1} voltage. However, the model accuracy is slightly lower for the 85 kHz oscillatory mode, which is caused by the parasitics in the LCS circuit (T_1, SA_{T1} and C_{T1}) and which determine peak voltage V_{T1}.

B. DC CB experimental results

Fig. 13 shows successful breaking of DC currents, when contacts separate at around the same time as T_1 turns off (t_{T1}=290 µs). Four different DC current commutation values are illustrated to confirm that the proposed DC CB can interrupt wide range of currents. The capacitor voltage (blue curve) indicates that UFD takes full 5 kV voltage stress. The UFD current (green curve) indicates interruption, while capacitor current (red current) indicates commutation to capacitor.

The test with the highest current shows 2100 A peak current, 1970 A current at the commutation, and 1650 A at the trip signal. The peak voltage stress across contacts is 5650 V.

The last column shows zoomed voltages around the commutation instant, and enables estimation of time t_e and changes in t_e with the magnitude of commutating current. At time t_e, V_{T1} and V_c curves separate and UFD takes voltage stress. The transistor (snubber) voltage keeps increasing for some time after T_1 turns off at t_{T1} indicating that UFD is still conducting. At the highest commutating DC current, the observed time t_e is 50-70 µs longer than t_{T1} which is similar as the settling time for the high frequency oscillations.

The highest value for steady-state transistor voltage is V_{T1}=350 V, which represents the theoretical value for the stress on LCS. This stress is similar as K150 arrester rating, however we have found that such arrester is inadequate as the timing margin is very narrow.

The time t_w can be labelled in Fig. 13d), considering that the arrester K385 begins to conduct at the voltage of 800 V, as can be seen in Fig. 11d). Therefore, we can determine the interval of t_w-t_e≈100 µs which gives theoretical window margin for setting timing of T_1. This is also safety margin to accommodate all inaccuracies in the contact assembly.

Fig. 13d) shows verification of PSCAD model. It enables accurate prediction of all variables including peak voltage stress V_{T1}, which is also shown in Fig. 3. However, this model cannot accurately estimate time t_e, since thermal arc phenomena are not included in the model.

The turquoise curve shows the arrester current I_{SA}, which gradually reduces and the residual breaker S_2 will finally interrupt the residual current.

C. Impact of different T_1 opening time t_{T1}

Fig. 14 shows unsuccessful DC current commutation, because of too late T_1 turning off (t_{T1}=330 µs). The problem with late T_1 timing is that arcing commences before T_1 turns off. We can conclude that UFD begins to arc because of the current drop (approximately 150A) visible around 40 µs before T_1 turns off, in Fig. 14(b). Current drops because of arc counter voltage. This arcing increases temperature of dielectric and reduces dielectric strength. Transistor T_1 opens at t_{T1} and current commutates to C_s but leakage current continues flowing through SA_{T1} maintaining UFD arc, as seen by the continuous rise of V_{T1} voltage according to V_c voltage, in Fig. 14(c). Once V_{T1} voltage reaches SA_{T1} saturation, UFD takes full current.

Fig. 15 shows unsuccessful current breaking because of too early T_1 turning off. The problem with such T_1 timing is that contact separation occurs too late in the zero-current window and therefore contact distance is inadequate to sustain voltage stress. UFD arc is broken and UFD takes some voltage stress but reignition occurs as seen in Fig. 15(c).

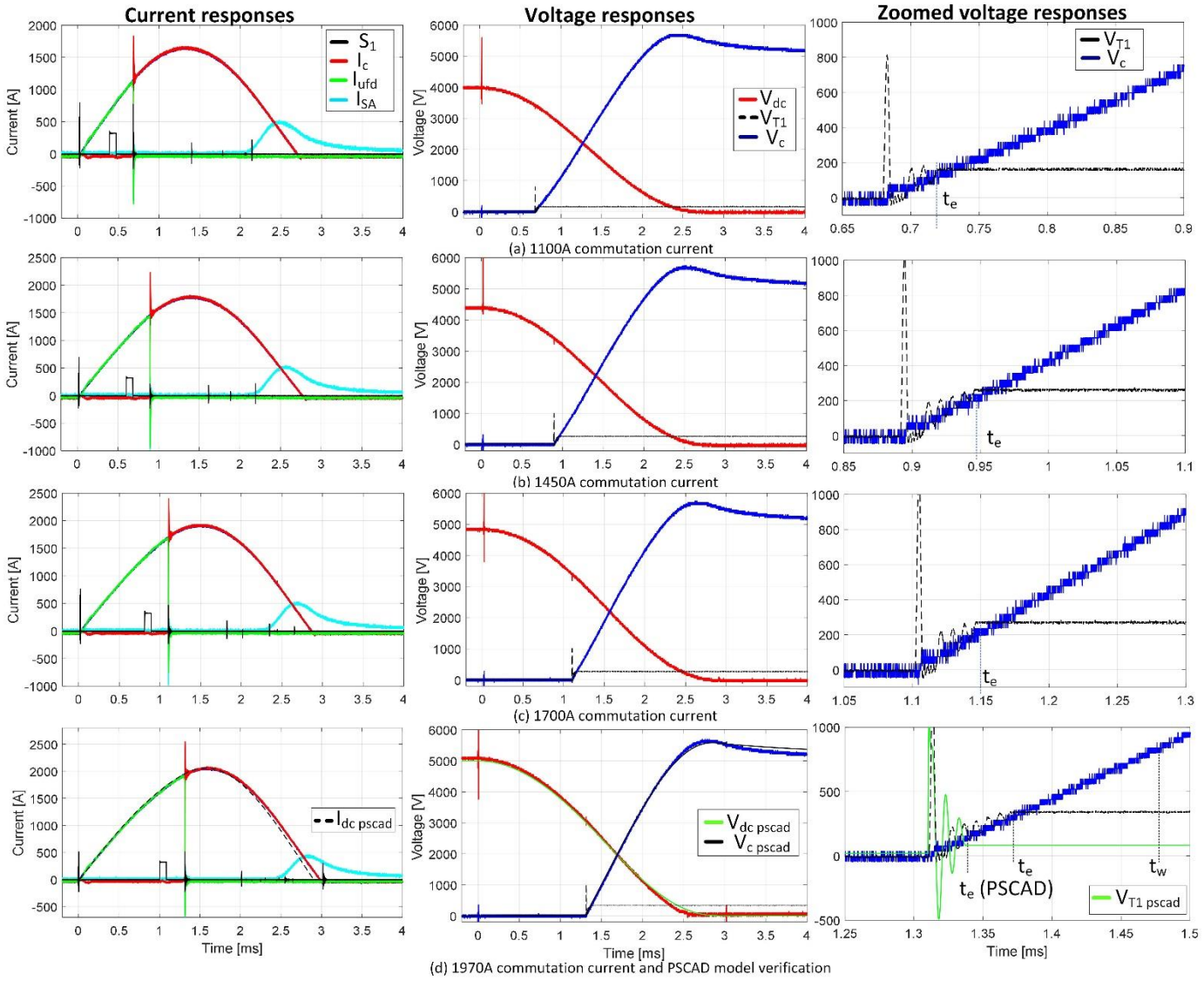

Fig. 13 Experimental responses for breaking 4 different DC current values (1100A, 1450A, 1700A and 1970A). PSCAD model verification shown in graphs d).

D. Parametric analysis of experimental results

Fig. 16 provides record of the tests with 6 different t_{T1}, and with 3 different SA_{T1}. We fixed a value for t_{T1} and then performed series of tests by gradually increasing fault current until unsuccessful breaking occurred. With even higher currents unsuccessful commutation always occurred, and with most parameters we did not continue testing once first failure occurred. The maximum successfully commutated current was reducing as we were moving away from the predicted contact separation time. At the delay of 330 µs, we were observing that notable arcing is present, (as illustrated in time-domain graphs in Fig. 14), and we have not increased delay further.

We obtained rated breaking current with 270 µs $<t_{T1}<$290 µs. It is concluded that the optimal t_{T1} is around the contacts separation time or slightly earlier. With K150 SA_{T1} arresters, we obtained the maximum commutating current of 1.7 kA while arresters K230 and K385 gave similar 2 kA current.

The results on hardware demonstrator give lower current and lower margin compared with the theoretical model. This is attributed to inferior manufacturing quality of UFD and contacts assembly in our laboratory (alignment precision, free play and materials used). Also, the parasitic inductances could be further reduced, as an example by using sandwich bus bars and wider cables.

Our testing has shown quite consistent successful breaking at the currents below the maximum interrupting value. With the proposed DC CB topology there is practically no arcing or very short arcing lasting below 50 µs. This eliminates or reduces thermal phenomena and makes results more consistent and predictable. Contrary, when disconnector arcing lasts for tens of milliseconds or longer, as when LCS is not used with disconnectors in the studies in [16], there is significant heating, larger inconsistency and probability for reignition.

VI. Scaling to Higher Voltages

It is meaningful to provide brief comparison with hybrid DC CB, considering possible upscaling for high voltage applications. It is assumed that UFD, LCS, and SA are identical, and only C_s replaces the main IGBT valve in a hybrid breaker.

In terms of performance, the proposed breaker inserts the counter voltage earlier. Similar benefits are expected as

analysed in detail in [14] and in [12], where it was concluded that commutation at the beginning of stroke reduces peak DC fault current and energy dissipation by around 30%.

Capacitors are convenient for series connection, and therefore the proposed DC CB topology enables good modularity and scalability (assuming that a module includes UFD, T_1 and C_s). Series connection of IGBTs on the other hand brings substantial grading and balancing challenges, although a single UFD can be used for HV DC CB.

We can also provide approximate cost comparison between capacitors and IGBT modules, based on our experience with component procurement. IGBTs require higher voltage margins, and approximately 3 series connected 4.5kV, IGBTs (Infineon FZ1800R45HL4S7BPSA1) would provide the same 6.5 kV voltage as C_s. The cost of the selected C_s capacitor is around 30% of the cost of these 3 IGBT modules (with drivers).

However, it is important to underscore that the design and operating margins are significantly smaller in the proposed CB.

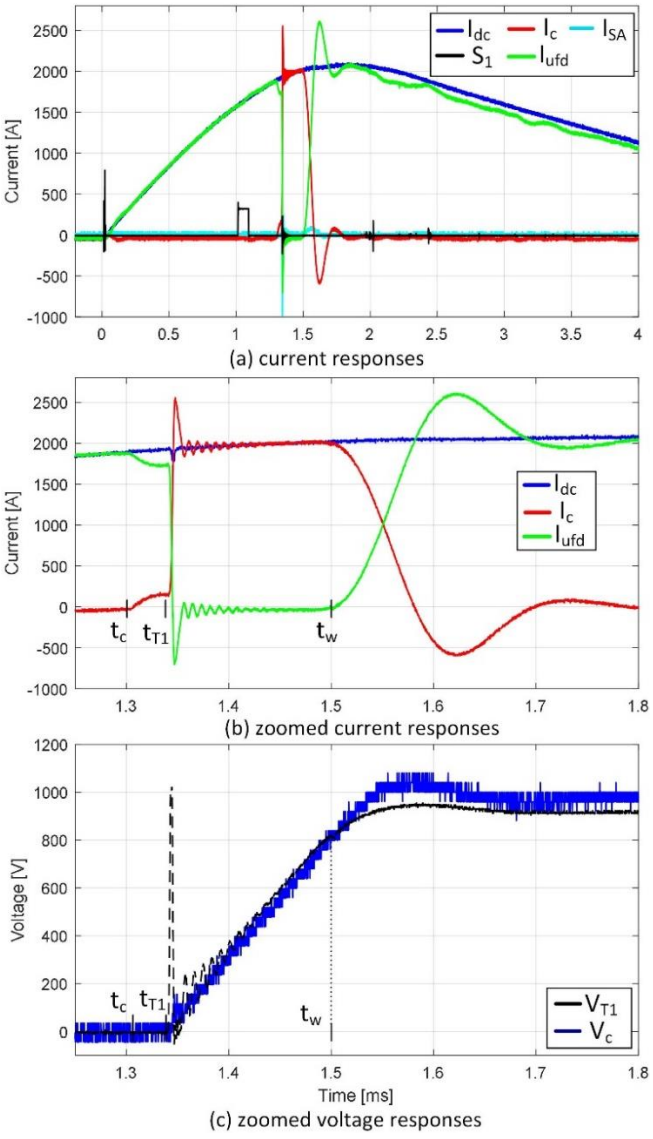

Fig. 14 Experimental responses of failed breaking at 1.9kA DC current because of too late T_1 opening.

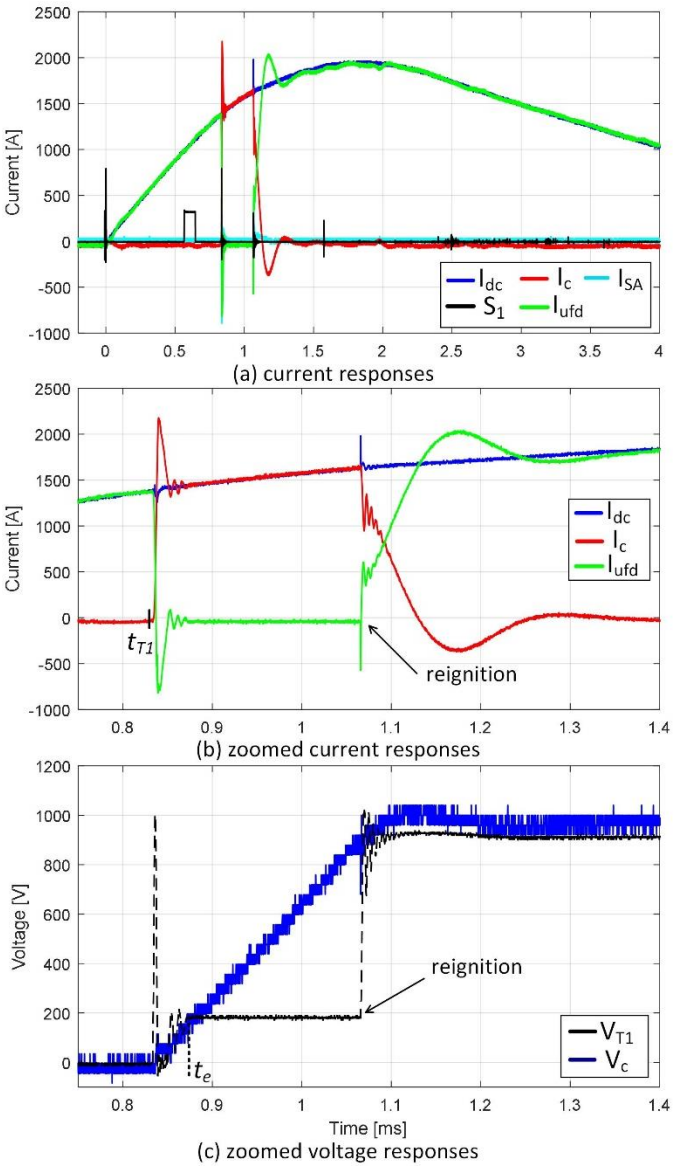

Fig. 15 Experimental responses of failed breaking at 1.4 kA DC current because of too early T_1 opening.

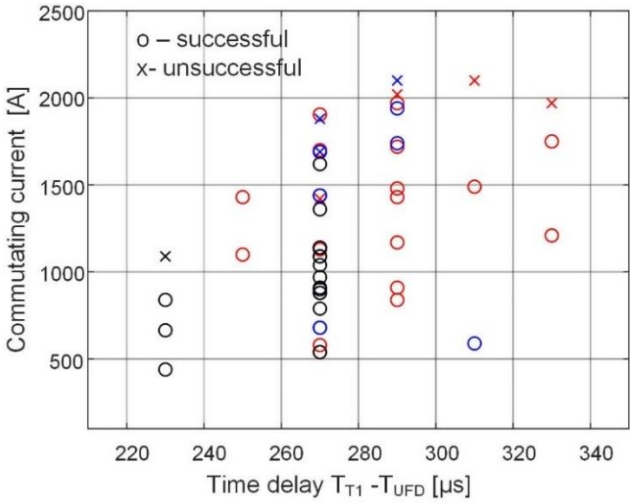

Fig. 16 Commutating current versus T_1 opening delay (T_{T1}-T_{UFD}). Red: K385 SA_{T1}, Blue: K230 SA_{T1}, and Black: K150 SA_{T1}.

VII. Conclusion

The article presents design, operation and experimental testing of a new type of mechanical DC CB with parallel capacitors. It is concluded that the topology offers advantages compared with hybrid DC CB in terms of performance and possibly costs. A detailed PSCAD model is presented and comparison with experimental results verifies model accuracy. A 5 kV, 2 kA hardware demonstrator with 1.5 ms opening time is developed in the university laboratory. The test results demonstrate successful breaking of a range of currents below the design value, with the measured time for insertion of capacitor voltage of around 290 µs. Further experimental analysis enables calculation of stresses on the key components and optimal timing for opening of LCS. The analysis of experimental results and PSCAD model concludes that there is around 100 µs theoretical margin for LCS opening time and contact inaccuracies to enable successful DC current breaking.

VIII. Acknowledgment

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